# Multisim™

## Component Reference Guide

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NATIONAL INSTRUMENTS™
ELECTRONICS WORKBENCH GROUP

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Multisim guides use the convention of an arrow (➢) to indicate the start of procedural information.

Multisim guides use the construction CTRL-KEY and ALT-KEY to indicate when you need to hold down the "Ctrl" or "Alt" key on your keyboard and press another key.

# The Multisim Documentation Set

Multisim documentation consists of the *User Guide*, the *Component Reference Guide* and online help. All Multisim users receive PDF versions of the *User Guide* and the *Component Reference Guide*.

You should also refer to *Getting Started with NI Circuit Design Suite*.

# Component Reference Guide

This guide contains information on the components found in Multisim.

The chapters in the *Component Reference Guide* are organized to follow the component groups that are found in the Multisim databases.

# Online Help

Multisim offers a full helpfile system to support your use of the product.

Choose **Help/Multisim Help** to display the helpfile that explains the Multisim program in detail, or choose **Help/Component Reference** to display the helpfile that contains details on the components families provided with Multisim. Both are compiled HTML helpfiles, offering a table of contents and index.

In addition, you can display context-sensitive help by pressing F1 from any command or window, or by clicking the **Help** button on any dialog box that offers it.

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## Appendix A


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# Chapter 1
# Source Components

## 1.1 Ground



A voltage measurement is always referenced to some point, since a voltage is actually a “potential difference” between two points in a circuit.

The concept of “ground” is a way of defining a point common to all voltages. It represents 0 volts. All voltage levels around the circuit are positive or negative when compared to ground. In power systems, the planet Earth itself is used for this reference point (most home power circuits are ultimately “grounded” to the Earth's surface for lightning protection). This is how the expression “earthing” or “grounding” a circuit originated.

Most modern power supplies have “floating” positive and negative outputs, and either output point can be defined as ground. These types of supplies can be used as positive (with respect to ground) or negative power supplies. In floating power supply circuits, the positive output is often used as the voltage reference for all parts of the circuit.

***Note*** Multisim supports a multipoint grounding system. Each ground connected is made directly to the ground plane.

### The Ground Component

This component has 0 voltage and so provides a clear reference point for calculating electrical values. You can use as many ground components as you want. All terminals connected to ground components represent a common point and are treated as joined together.

Not all circuits require grounding for simulation; however, any circuit that uses an opamp, transformer, controlled source or oscilloscope must be grounded. Also, any circuit which contains both analog and digital components should be grounded. If a circuit is ungrounded or improperly grounded (even if it does not need grounding in reality), it may not be simulated. If it is simulated, it may produce inconsistent results. The linear transformer must be grounded on both sides.

# 1.2 Digital Ground



The digital ground is used to ground digital components which do not have an explicit ground pin. The digital ground must be placed on the schematic but does not need to be connected directly to any component.

***Tip*** If you are unsure of the ground required for a digital component that has its ground pin hidden, double-click on the component and click on the **Pins** tab. Locate GND in the **Name** column and move across to the **Net** column. In most cases, the name of the net will be GND.

The default Reference Designator (RefDes) for the digital ground is GND. When you connect a wire to a digital ground, the wire's net name will be the same as the digital ground's RefDes. Multiple instances of a digital ground may be placed on a schematic but there will only be one matching net in the schematic.

If you rename a digital ground by changing its RefDes, and there are other instances of the digital ground with the same RefDes on the schematic, you will be prompted to confirm that you want to change all instances of the RefDes. If you select No, only the RefDes for the selected digital ground will change. Remember that if a digital ground's RefDes is changed, the net name of any wires attached to it will change to match the new RefDes. For a more detailed discussion, see "Global Nets" in the *Multisim User Guide*, or the Multisim helpfile.

➢ To change the RefDes of a digital ground:

1. Double-click on the component to display its properties dialog box, and click on the **Label** tab.
2. Change the entry in the **RefDes** field and click **OK** to close the dialog box.

# 1.3 DC Voltage Source (Battery)




## Battery Background Information

A battery may be a single electrochemical cell or a number of electrochemical cells wired in series. It is used to provide a direct source of voltage and/or current.

A single cell has a voltage of approximately 1.5 volts, depending on its construction. It consists of a container of acid in which an electrode is placed. Chemical action causes electrons to flow between the electrode and the container, and this creates a potential difference between the electrode and the material of the container.

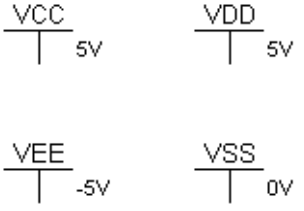
Batteries can be rechargeable and can be built to deliver extremely high currents for long periods. The automobile ignition battery is an application of a battery as a “current source”; the voltage may vary considerably under use, with no visible battery deterioration.

Batteries may be used as voltage references, their voltage remaining stable and predictable to many figures of accuracy for many years. The standard cell is such an application. A standard cell is a voltage source, and it is important that current is not drawn from the standard cell.

### Battery Component

Multisim includes both an ideal battery (DC_POWER), with no internal resistance and a non-ideal battery, that allows you to changes its internal resistance and capacity (in ampere hours).

## 1.4 Digital Power Supplies




The Power Source component family includes the digital power supplies VCC, VDD, VEE, and VSS. These are used to connect power to digital components which do not have an explicit power pin on their symbol. They can also be wired directly into a circuit as desired.

***Tip*** If you are unsure of the power supply required for a digital component that has its power pin hidden, double-click on the component and click on the **Pins** tab. Locate the power supply in the **Name** column. Some components, will have more than one power supply (for example, a CMOS 4522BD has both VDD and VSS).

When you connect a wire to a digital power supply (for example, VCC), the wire’s net name will be the same as the digital supply’s RefDes (so in the case of VCC, the net name will be VCC). Multiple instances of a digital power supply may be placed on a schematic but there will only be one matching net in the schematic. Also, when you change a digital power supply’s voltage, the voltage for all instances of that power supply on the schematic will change to reflect the new setting.

If you rename a digital power supply by changing its RefDes, and there are other instances of the same supply on the schematic, you will be prompted to confirm that you want to change all instances of the RefDes. If you select No, only the RefDes for the selected component will change. Remember that if a digital power supply's RefDes is changed, the net name of any wires attached to it will change to match the new RefDes. For a more detailed discussion, see "Global Nets" in the *Multisim User Guide*, or the Multisim helpfile.

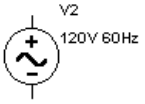
- To change the properties of a digital power supply:
  1. Double-click on the component to display its properties dialog box, and click on the **Value** tab. Change the value in the **Voltage (V)** field as desired.
  2. To change the reference designator for the component, click on the **Label** tab and change the entry in the **RefDes** field.
  3. Click **OK** to close the dialog box.

# 1.5 DC Current Source




The current generated by this source can be adjusted from microamps to kiloamps.

# 1.6 AC Voltage Source




The root-mean-square (RMS) voltage of this source can be adjusted from µV to kilovolts. You can also control its frequency and phase angle.

$$V_{RMS} = \frac{V_{peak}}{\sqrt{2}}$$

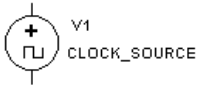
# 1.7 AC Current Source




The RMS current of this source can be adjusted from microamps to kiloamps. You can also control its frequency and phase angle.

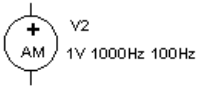
$$I_{RMS} = \frac{I_{peak}}{\sqrt{2}}$$

# 1.8 Clock Source




This component is a square wave generator. You can adjust its voltage amplitude, duty cycle and frequency.

# 1.9 Amplitude Modulation (AM) Source




The AM source (single-frequency amplitude modulation source) generates an amplitude-modulated wave. It can be used to build and analyze communications circuits.

## 1.9.1 Characteristic Equation

The behavior of the AM source is described by:

$$V_{OUT} = vc * \sin(2 * \pi * fc * TIME) * (1 + m * \sin(2 * \pi * fm * TIME))$$

where:

vc = carrier amplitude, in volts

fc = carrier frequency, in hertz

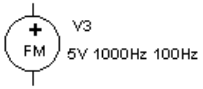
m = modulation index

fm = modulation frequency, in hertz

# 1.10 FM Source

The FM source (single-frequency frequency modulation source) generates a frequency-modulated wave. It can be used to build and analyze communications circuits.The signal output can be either a current source or a voltage source.

## 1.10.1 FM Voltage Source




This is an FM source of which the output is measured in voltage.

## 1.10.2 Characteristic Equation

The behavior of the FM voltage source is described by:

$$V_{OUT} = va * \sin(2 * \pi * fc * TIME + m * \sin(2 * \pi * fm * TIME))$$

where:

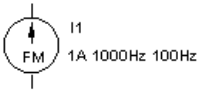
va = peak amplitude, in volts

fc = carrier frequency, in Hz

m = modulation index

fm = modulation frequency, in Hz

## 1.10.3 FM Current Source

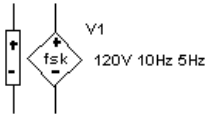



This component is the same as the FM voltage source, except that the output is measured in current.

## 1.10.4 Characteristic Equation

The behavior of the FM current source is described by the same equation as in the FM Voltage Source, with Vout replaced by Iout.

# 1.11 FSK Source



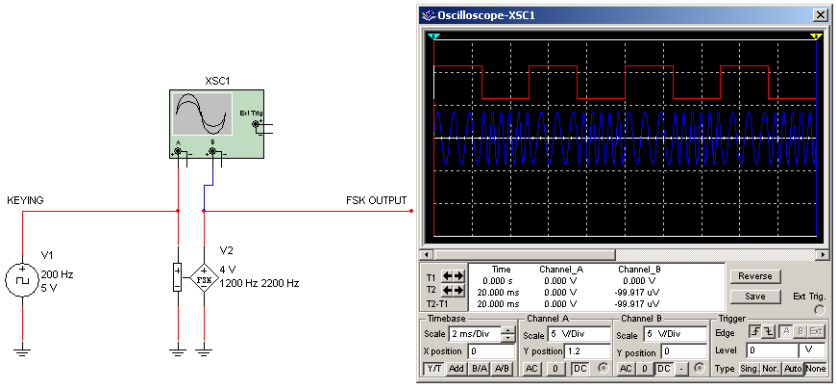

This source is used for keying a transmitter for telegraph or teletype communications by shifting the carrier frequency over a range of a few hundred hertz. The frequency shift key (FSK) modulated source generates the mark transmission frequency, f1, when a binary 1 is sensed at the input, and the space transmission frequency, f2, when a 0 is sensed.

FSK is used in digital communications systems such as in low speed modems (for example, a Bell 202 type modem - 1200 baud or less).

In this system, a digital high level is referred to as a MARK and is reproduced as a frequency of 1200 Hz. A digital low level is referred to as a SPACE and is represented by a frequency of 2200 Hz.

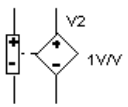
In the example shown below, the frequency shift keying signal is a 5v (TTL) square wave.

When the keying input is 5V, a MARK frequency of 1200 Hz is output. When keying voltage is 0V, a SPACE frequency of 2200 Hz is output.




This component is a square wave generator. You can adjust its voltage amplitude, duty cycle and frequency.

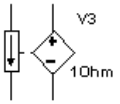
# 1.12 Voltage-Controlled Voltage Source




The output voltage of this source depends on the voltage applied to its input terminal. The ratio of the output voltage to the input voltage determines its voltage gain (E). Voltage gain can have any value from mV/V to kV/V.

$$E = \frac{V_{OUT}}{V_{IN}}$$

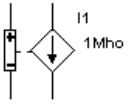
# 1.13 Current-Controlled Voltage Source




The output voltage of this source depends on the current through the input terminals. The two are related by a parameter called transresistance (H), which is the ratio of the output voltage to the input current. It can have any value from mW to kW.

$$H = \frac{V_{OUT}}{I_{IN}}$$

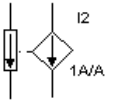
# 1.14 Voltage-Controlled Current Source




The output current of this source depends on the voltage applied at the input terminals. The two are related by a parameter called transconductance (G), which is the ratio of the output current to the input voltage. It is measured in mhos (also known as seimens) and can have any value from mmhos to kmhos.

$$G = \frac{I_{OUT}}{V_{IN}}$$

# 1.15 Current-Controlled Current Source

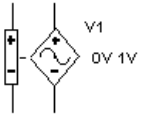



The magnitude of the current output of a current-controlled current source depends on the current through the input terminals. The two are related by a parameter called current gain (F),

which is the ratio of the output current to the input current. The current gain can have any value from mA/A to kA/A.

$$F = \frac{I_{OUT}}{I_{IN}}$$

# 1.16 Voltage-Controlled Sine Wave




This oscillator takes an input AC or DC voltage, which it uses as the independent variable in the piecewise linear curve described by the (control, frequency) pairs. From the curve, a frequency value is determined, and the oscillator outputs a sine wave at that frequency. When only two co-ordinate pairs are used, the oscillator outputs a linear variation of the frequency with respect to the control input. When the number of co-ordinate pairs is greater than two, the output is piecewise linear. You can change the peak and valley values of the output sine wave by resetting the Output peak high value and Output peak low value on the model parameter dialog box.

## Example

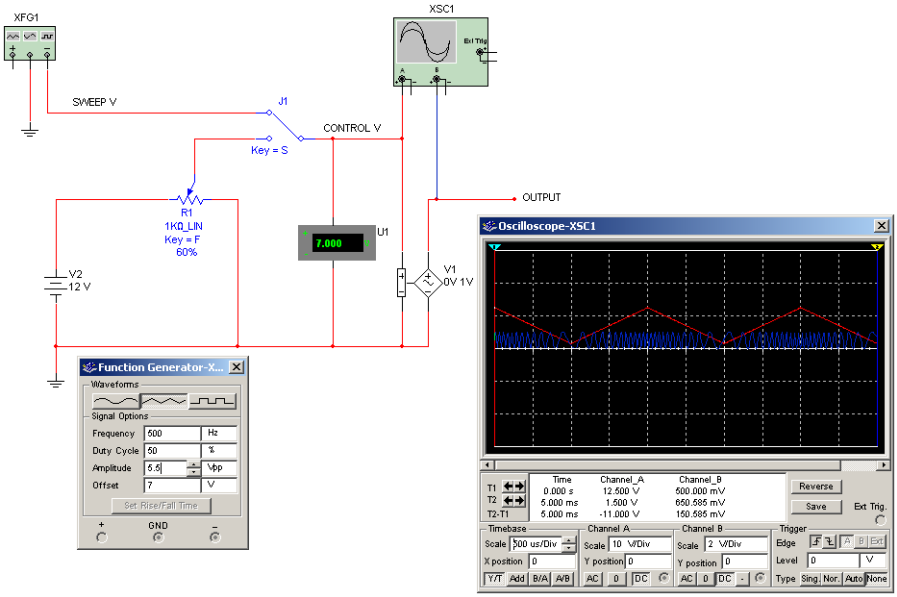
The example shows a sine wave generator with output frequency determined by a control voltage.

Control voltage may be DC, controlled by a potentiometer, as is the case for many signal generators and function generators, or may be the output from a PLL that determines a precise frequency.

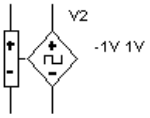
Control voltage may be a continuous variable of any desired shape as required in sweep generators and spectrum analysers.

In the example shown below, the VCO parameters are set so that control voltage of 0V produces an output frequency of 100Hz and a control voltage of 12V produces an output frequency of 20KHz.

A square wave control voltage produces a form of FSK (frequency shift keying), a sine wave control voltage produces a form of FM (frequency modulation).




# 1.17 Voltage-Controlled Square Wave




This oscillator is identical to the voltage-controlled sine wave oscillator except that it outputs a square wave. This oscillator takes an input AC or DC voltage, which it uses as the independent variable in the piecewise linear curve described by the (control, frequency) pairs. From the curve, a frequency value is determined, and the oscillator outputs a square wave at that frequency. When two co-ordinate pairs are used, the oscillator outputs a linear variation of the frequency with respect to the control input. When the number of co-ordinate pairs is greater than two, the output is piecewise linear. You can change duty cycle, rise and fall times, and the peak and valley values of the output square wave by resetting the Output peak high value and Output peak low value on the model parameter dialog box.

## Example

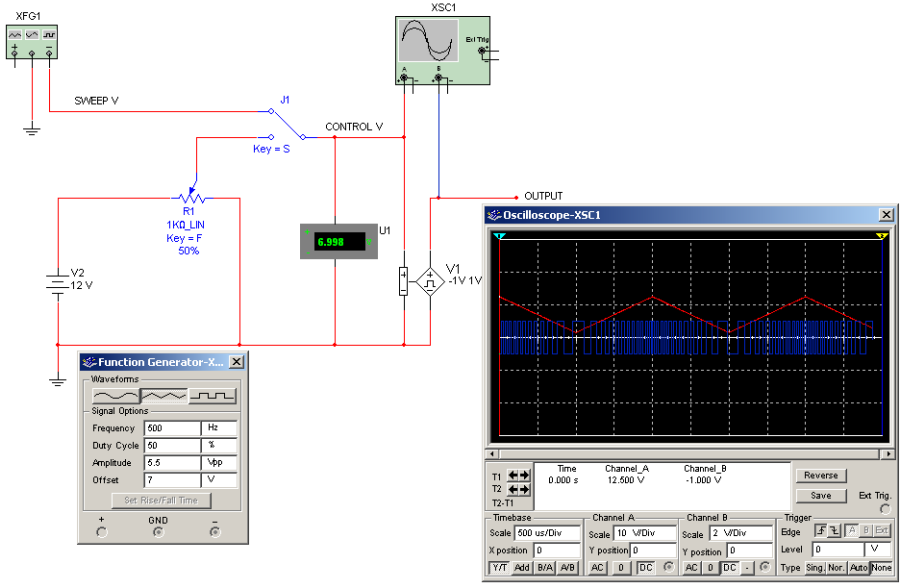
The example shows a square wave generator with output frequency determined by a control voltage.

Control voltage may be DC, controlled by a potentiometer, as is the case for many signal generators and function generators.

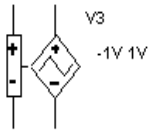
Control voltage may be a continuous variable of any desired shape as required in sweep generators and spectrum analysers.

In the example shown below, the VCO parameters are set so that control voltage of 0V produces an output frequency of 100Hz and control voltage of 12V produces an output frequency of 20KHz.

A square wave control voltage produces a form of FSK (frequency shift keying), a sine wave control voltage produces a form of FM (frequency modulation).



# 1.18 Voltage-Controlled Triangle Wave




This oscillator is identical to the voltage-controlled sine wave oscillator except that it outputs a triangle wave. This oscillator takes an input AC or DC voltage, which it uses as the independent variable in the piecewise linear curve described by the (control, frequency) pairs. From the curve, a frequency value is determined, and the oscillator outputs a triangle wave at that frequency. When two co-ordinate pairs are used, the oscillator outputs a linear variation of the frequency with respect to the control input. When the number of co-ordinate pairs is greater than two, the output is piecewise linear. You can change the rise time duty cycle and the peak and valley values of the output triangle wave by resetting the Output peak high value and Output peak low value on the model parameter dialog box.

## Example

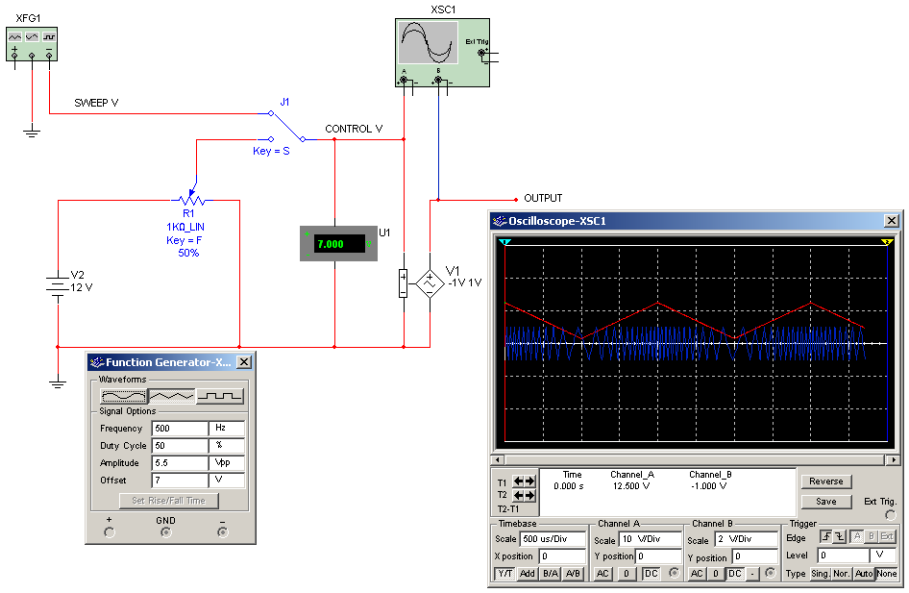
The example shows a triangle wave generator with output frequency determined by a control voltage.

Control voltage may be DC, controlled by a potentiometer, as is the case for many signal generators and function generators.

Control voltage may be a continuous variable of any desired shape as required in sweep generators and spectrum analysers.

In the example shown below, the VCO parameters are set so that control voltage of 0V produces an output frequency of 100Hz and control voltage of 12V produces an output frequency of 20KHz.

A square wave control voltage produces a form of FSK (frequency shift keying), a sine wave control voltage produces a form of FM (frequency modulation).




# 1.19 Voltage-Controlled Piecewise Linear Source

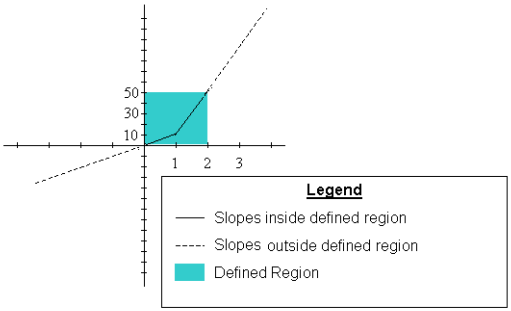



This source (voltage-controlled piecewise linear source) allows you to control the shape of the output waveform by entering up to five (input, output) pairs, which are shown in the **Value** tab of the component's properties dialog box as (X,Y) co-ordinates.

The X values are input co-ordinate points and the associated Y values represent the outputs of those points. If you use only two pairs, the output voltage is linear.

Outside the bounds of the input co-ordinates, the source extends the slope found between the lowest two co-ordinate pairs and the highest two co-ordinate pairs. A potential effect of this behavior is that it can unrealistically cause the output to reach a very large or very small value,

especially for large input values. Therefore, keep in mind that this source does not inherently provide a limiting capability.




The graph above is a result of the following co-ordinates entered into the voltage-controlled piecewise linear source are as follows:

| x-array | y-array |
|---|---|
| 0 | 0 |
| 1 | 10 |
| 2 | 50 |

In order to reduce the potential for non-convergence of simulations, the source provides for smoothing around the co-ordinate pairs. If **Input smoothing domain** (ISD) is set to, say, 10%, the simulator assumes a smoothing radius about each co-ordinate point equal to 10% of the length of the smaller of the segments above and below each co-ordinate point.

# 1.20 Piecewise Linear Source

The Piecewise Linear Source (PWL) is available as either a voltage source or a current source.

This source allows you to control the shape of the waveform by entering pairs of time and voltage/current values. Each pair specifies the value of the source at the specified time. At intermediate values of time, the value of the source is determined by linear interpolation.

The component also reads a specified file which contains a table of time and current or voltage points. Using the data in the table, the component generates a current or voltage waveform specified by the input text file.

➢ To set up the PWL source:

1. Double-click on the PWL Source to open its properties dialog box.
2. From the **Value** tab, either select the file containing the time and voltage or current points from the dialog box or enter the data points manually.

   Refer to the following for details on each type of PWL Source:

   - “Piecewise Linear Voltage Source” on page 1-17
   - “Piecewise Linear Current Source” on page 1-17.

## 1.20.1 PWL Source Input Text File Specification

This file must contain a list of time and voltage or current points. Each line of the file represents one point. The format is:

Time <space(s)> Voltage *or* Time <space(s)> Current

You can leave any amount of space between the *Time* and *Voltage/Current* fields. Here is an example of an ideally formatted input file:

```
0             0
2.88e-06      0.0181273
5.76e-06      0.0363142
1e-05         0.063185
1.848e-05     0.117198
```

| If the PWL source encounters... | It will... |
|---|---|
| non-whitespace at beginning of line | ignore the line |
| non-numeric data following correctly formatted data | accept data, ignore non-numeric data |
| non-whitespace between *Time* and *Voltage/Current* | ignore the line |
| whitespace preceding correctly formatted data | accept data, ignore whitespace |

Please note the following special considerations:

- If the earliest input point is not at time 0.0, then the PWL source gives the output of the earliest time point from time 0.0 to that earliest time.
- After the latest input point, the PWL source gives the output of the latest time point in the file from that latest time until the simulation ends.
- Between input points, the PWL source uses linear interpolation to generate output.
- The PWL source can handle unsorted data. It sorts the points by time before the simulation starts.

## 1.20.2 Piecewise Linear Voltage Source



This component is a piecewise linear source with a voltage output.

The **Value** tab in this component's properties dialog box contains the following:

- The **Use data directly from file** radio button, used if your data pairs are in a separate `.txt` file. If you choose this option, the circuit will depend on the text file. When this button is selected the following become active:
  - **Filename** — click on the button to the right of this field and navigate to the data file. The data file must have a `.txt` extension to be used.

***Note*** If you do not specify a filename, the PWL voltage source behaves like a short circuit. An error message does not display in this case.

  - **Edit file** — click to open the data file for editing.
- The **Enter data points in table** radio button, used if you wish to manually enter the data pairs, without referencing an external file. If you choose this option, the following become active:
  - **Time** and **Voltage** columns — where you enter the desired time and voltage data points.
  - **Initialize from file** — click to view the data pairs from a specific file. If you choose this option, the circuit will not depend on the text file. The data points will be loaded and saved into the circuit file.
- **Repeat data during simulation** — enable to continuously run the file during simulation. If this checkbox is not enabled, output from the source will cease once the final data pair has been read.

## 1.20.3 Piecewise Linear Current Source



This component is a piecewise linear source with a current output.

The **Value** tab in this component's properties dialog box contains the following:

- The **Use data directly from file** radio button, used if your data pairs are in a separate `.txt`

file. If you choose this option, the circuit will depend on the text file. When this button is selected the following become active:

- **Filename** — click on the button to the right of this field and navigate to the data file. The data file must have a `.txt` extension to be used.

***Note*** If you do not specify a filename, the output of the PWL current source behaves like an open circuit. An error message does not display in this case.

- **Edit file** — click to open the data file for editing.

- The **Enter data points in table** radio button, used if you wish to manually enter the data pairs, without referencing an external file. If you choose this option, the following become active:
  - **Time** and **Current** columns — where you enter the desired time and current data points.
  - **Initialize from file** — click to view the data pairs from a specific file. If you choose this option, the circuit will not depend on the text file. The data points will be loaded and saved into the circuit file.
- **Repeat data during simulation** — enable to continuously run the file during simulation. If this checkbox is not enabled, output from the source will cease once the final data pair has been read.

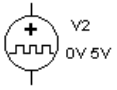
# 1.21 Pulse Source

This source includes pulse voltage source and pulse current source.The Pulse sources are configurable sources whose output can be set to produce periodic pulses.

The following parameters can be modified:

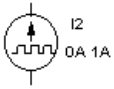
- Initial Value
- Pulsed Value
- Delay time
- Rise Time
- Fall time
- Pulse Width
- Period

## 1.21.1 Pulse Voltage Source



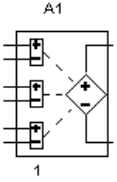

This component is a pulse source of which the output is measured in voltage.

## 1.21.2 Pulse Current Source




This component is the same as the Pulse Voltage Source, except that the output is measured in current.

# 1.22 Polynomial Source




This is a voltage-controlled voltage source defined by a polynomial transfer function. It is a specific case of the more general nonlinear dependent source. Use it for analog behavioral modeling.

The polynomial source has three controlling voltage inputs, namely, $V_1$, $V_2$ and $V_3$.

### Output Voltage Characteristic Equation

The output voltage is given by:

$$V_{OUT} = A + B*V_1 + C*V_2 + D*V_3 + E*V_1^2 + F*V_1*V_2 + G*V_1*V_3 + H*V_2^2 + I*V_2*V_3 + J*V_3^2 + K*V_1*V_2*V_3$$

where:

A = constant

B = coefficient of $V_1$

C = coefficient of $V_2$

D = coefficient of $V_3$

E = coefficient of $V_{1^2}$

F = coefficient of $V_1 * V_2$

G = coefficient of $V_1 * V_3$

H = coefficient of $V_{2^2}$

I = coefficient of $V_2 * V_3$

J = coefficient of $V_{3^2}$

K = coefficient of $V_1 * V_2 * V_3$

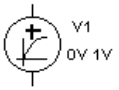
# 1.23 Exponential Source

The exponential sources are configurable sources whose output can be set to produce an exponential signal.

The following parameters can be modified:

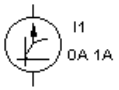
- Initial Value
- Pulsed Value
- Rise Delay time
- Rise Time
- Fall Delay time
- Fall Time

## 1.23.1 Exponential Voltage Source




This component is an exponential source of which the output is measured in voltage.

## 1.23.2 Exponential Current Source




This component is the same as the Exponential Voltage Source, except that the output is measured in current.

# 1.24 Nonlinear Dependent Source

Use this source for analog behavioral modeling. This generic source allows you to create a sophisticated behavioral model by entering a mathematical expression.

This source uses analog behavioral modeling through mathematical expressions.

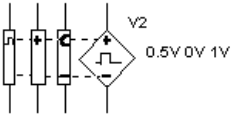
The output voltage or current can be a function of up to four voltages and two currents. Voltages and currents are referenced by connecting the input pins of this device to schematic nodes.

For a more flexible solution, see “ABM Sources” on page 1-49.

- To change the nonlinear dependent source’s value:
  1. Double-click on the placed component and click the **Value** tab.
  2. Complete the **Source Expression**.

***Note*** If you set the dependent variable to “V”, the output is in voltage; if you set it to “I”, the output is in current.

# 1.25 Controlled One-Shot

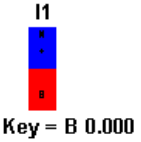



This oscillator takes an AC or DC input voltage, which it uses as the independent variable in the piecewise linear curve described by the (control, pulse width) pairs. From the curve, a pulse width value is determined, and the oscillator outputs a pulse of that width. You can

change clock trigger value, output delay from trigger, output delay from pulse width, output rise and fall times, and output high and low values.

When only two co-ordinate pairs are used, the oscillator outputs a linear variation of the pulse with respect to the control input. When the number of co-ordinate pairs is greater than two, the output is piecewise linear.

# 1.26 Magnetic Flux Source




This device is used with a Hall Effect Sensor.

The Magnetic Flux Source uses the “B” key to change the density and polarity of the magnetic flux impacting on a Hall Effect Sensor. You must specify the sphere of influence of the magnetic flux source by entering an integer value in the Magnetic Channel field in the Value tab of the component’s properties screen.

The Magnetic Channel field on the Hall Effect Sensor must have a matching integer value for that sensor to be influenced by the source. No two magnetic flux sources or generators should have the same integer value in the Magnetic Channel field. You can have as many Hall Effect Sensors as you wish to react to any given source/generator and as many different sources/generators as desired as long as each source/generator has a different integer value.

# 1.27 Magnetic Flux Generator

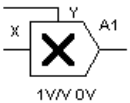



This device is used with a Hall Effect Sensor.

The Magnetic Flux Generator produces a continuous varying magnetic field (sinusoidal with N and S peaks). You can define the flux density, rate of rotation (translating to frequency) and specify the sphere of influence of the generator by putting a unique integer value in the Magnetic Channel field in the Value tab of the source’s properties screen.

The Magnetic Channel field on the Hall Effect Sensor must have a matching integer value for that sensor to be influenced by the generator. No two magnetic flux generators or sources should have the same integer value in the Magnetic Channel field. You can have as many Hall Effect Sensors as you wish to react to any given source/generator and as many different sources/generators as desired as long as each source/generator has a different integer value.

# 1.28 Multiplier




This component multiplies two input voltages.

The basic function multiplies the X and Y inputs.

Vo = Vx * Vy

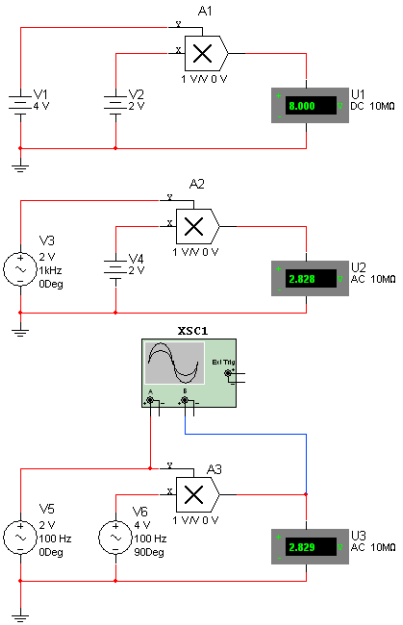
Gain factors may be applied to the X and Y inputs and to the output.

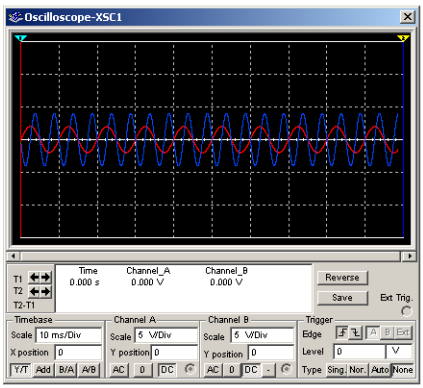
Examples shown below:

a) Two DC voltages are multiplied (4V * 2V = 8V)

b) Two volts DC multiplied by 2 V peak

c) Two AC signals




## Characteristic Equation

The output voltage is given by:

$$V_{out} = K\left( X_K\left(V_x + X_{off}\right) * Y_k\left(V_y + Y_{off}\right)\right) + off$$

where:

$V_x$ = input voltage at x

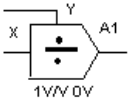
$V_y$ = input voltage at y

Other symbols used in these equations are defined in “Multiplier Parameters and Defaults”.

### Multiplier Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| k | Output gain | 0.1 | V/V |
| off | Output | 0.0 | V |
| Yoff | Y offset | 0.0 | V |
| Yk | Y gain | 1.0 | V/V |
| Xoff | X offset | 0.0 | V |
| Xk | X gain | 1.0 | V/V |

# 1.29 Divider




This component divides one voltage (the y input, or numerator) by another (the x input, or denominator).

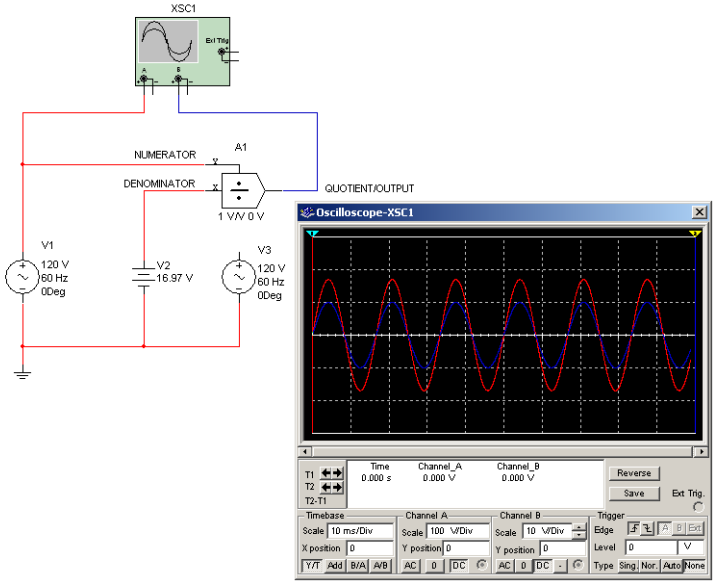
Vo = Vy/Vx

You can limit the value of the denominator input to a value above zero by using the parameter XLowLim. This limit is approached through a quadratic smoothing function, the domain of which you can specify as an absolute value in XDS.

In the example shown below, the 120v RMS (339.38v peak to peak) sine wave at the Y input is divided by a 16.96V DC voltage at the X input. The result is 339.38v (peak to peak) / 16.97V = 20v peak to peak.

If Vx is replaced with a 12v RMS voltage, in phase with Vy, the output will be 10V DC.

CAUTION If the X (denominator) voltage crosses 0v when any voltage is present at the Y (numerator) terminal, the quotient will go to infinity and a large positive or negative “spike” will be observed on the scope.




## Characteristic Equation

$$V_{out} = \left( \frac{\left(V_y + Y_{off}\right) * Y_k}{\left(V_x + X_{off}\right) * X_k} \right) * k + off$$

where:

$V_x$ = input voltage at x

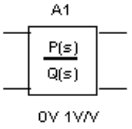
$V_y$ = input voltage at y

Other symbols used in these equations are defined in the table below.

### Divider Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| k | Output gain | 1 | V/V |
| off | Output offset | 0 | V |
| Yoff | Y (Numerator) offset | 0 | V |
| Yk | Y (Numerator) gain | 1 | V/V |
| Xoff | X (Denominator) offset | 0 | V |
| Xk | X (Denominator) gain | 1 | V/V |
| XLowLim | X (Denominator) lower limit | 100 | pV |
| XSD | X (Denominator) smoothing domain | 100 | pV |

# 1.30 Transfer Function Block




This component models the transfer characteristic of a device, circuit or system in the s domain. The transfer function block is specified as a fraction with polynomial numerators and denominators. A transfer function up to the third order can be directly modeled. This component may be used in DC, AC and transient analyses.

## Characteristic Equation

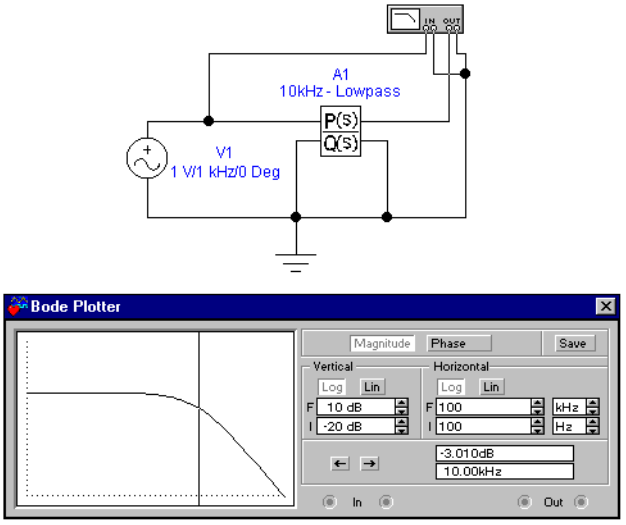
This transfer function model is defined in a form of the rational function:

$$T(s) = \frac{Y(s)}{X(s)} = K * \frac{A_3 s^3 + A_2 s^2 + A_1 s + A_0}{B_3 s^3 + B_2 s^2 + B_1 s + B_0}$$

Transfer functions up to the third order may be modeled.

In the example shown below, the transfer function for a simple first order low pass filter is used. Only the numerator and denominator constants A0 and B0 are required in this case. These are equal to two pi times the cutoff frequency (first pole).

The cursor on the Bode Plotter may be used to confirm first order performance with -3dB at 10kHz. and rolloff of 6dB per octave above 20kHz.

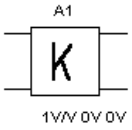



## Transfer Function Block Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| VIoff | Input voltage offset | 0 | V |
| K | Gain | 1 | V/V |
| VINT | Integrator stage initial conditions | 0 | V |
| w | Denormalized corner frequency | 1 | - |
| A3 | Numerator 3rd order coefficient | 0 | - |
| A2 | Numerator 2nd order coefficient | 0 | - |
| A1 | Numerator 1st order coefficient | 0 | - |
| A0 | Numerator constant | 1 | - |

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| B3 | Denominator 3rd order coefficient | 0 | - |
| B2 | Denominator 2nd order coefficient | 0 | - |
| B1 | Denominator 1st order coefficient | 0 | - |
| B0 | Denominator constant | 1 | - |

# 1.31 Voltage Gain Block



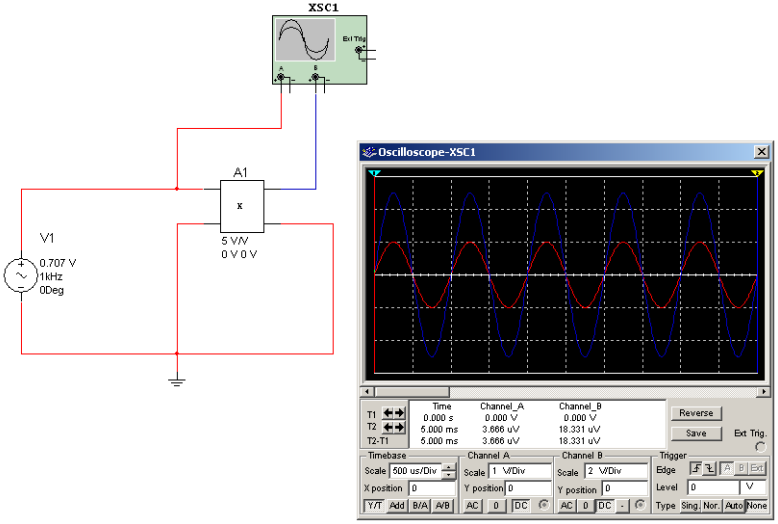

This component multiplies the input voltage by the gain and delivers it to the output. This represents a voltage amplifier function with the gain factor, K, selectable with the Value tab of the component's properties screen. The voltage gain block is used in control systems and analog computing applications.

In the example shown below, the input is a 0.707v RMS (2v peak to peak) sine wave and the gain factor K is set at 5. The output then is K times the input.

(.707*5= 3.535v RMS or 10 v peak to peak)

**Caution** Using the default model, as in this example, sine wave inputs may be any value.

Suitable settings of model parameters will allow for virtually unlimited flexibility for practical applications.



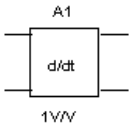

## Characteristic Equation

$$V_{out} = K(V_{in} + V_{Ioff}) + V_{Ooff}$$

## Voltage Gain Block Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| K | Gain | 1 | V/V |
| VIoff | Input offset voltage | 0 | V |
| VOoff | Output offset voltage | 0 | V |

# 1.32 Voltage Differentiator




This component calculates the derivative of the input voltage (the transfer function, s) and delivers it to the output. It is used in control systems and analog computing applications.

Differentiation may be described as a “rate of change” function and defines the slope of a curve.

Rate of change = dV/dT

## Characteristic Equation

$$V_{out}(t) = K\frac{dV_i}{dt} + V_{Ooff}$$

## Voltage Differentiator Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| K | Gain | 1 | V/V |
| VOoff | Output offset voltage | 0 | V |
| Vl | Output voltage lower limit | -1e+12 | V |
| Vu | Output voltage upper limit | 1e+12 | V |
| Vs | Upper and lower smoothing range | 1e-06 | V |

# 1.32.1 Investigations

## Sine wave

The slope of a sine wave changes continuously and smoothly. Therefore, the differentiator output should follow the sine shape.

In the example circuit shown below, if you change frequency from 10Hz. to 100Hz., the rate of change of the waveform will increase by a factor of 10. The differentiator output will also increase by the same factor. When investigating, note also a 90 degree phase shift from input to output.

## Triangle waveforms

In an ideal triangle waveform the rising and falling slopes are constant with an abrupt change taking place at the peaks.

Since the rate of change (slope) during rise and fall are constant, the differential result is also constant.

The reversal of slope at the peaks (from rise to fall/fall to rise) produces a large instantaneous change in the differentiator output, resulting in a square wave output.

In the example circuit, as for the sine wave, if you change frequency from 10Hz. to 100Hz., the rate of change of the waveform will increase by a factor of 10. The differentiator output will also increase by the same factor.

## Square waves

In an ideal square wave, the change takes place only at the rising and falling edges. The change is instantaneous. This instantaneous rate of change

(dV/dT = dV/0)

will produce an infinitely large output from a differentiator.

Since ideal square or pulse waveforms, as produced by the function generator in Multisim, have zero rise and fall times, the result of differentiation is infinite (dV/0 = infinity).

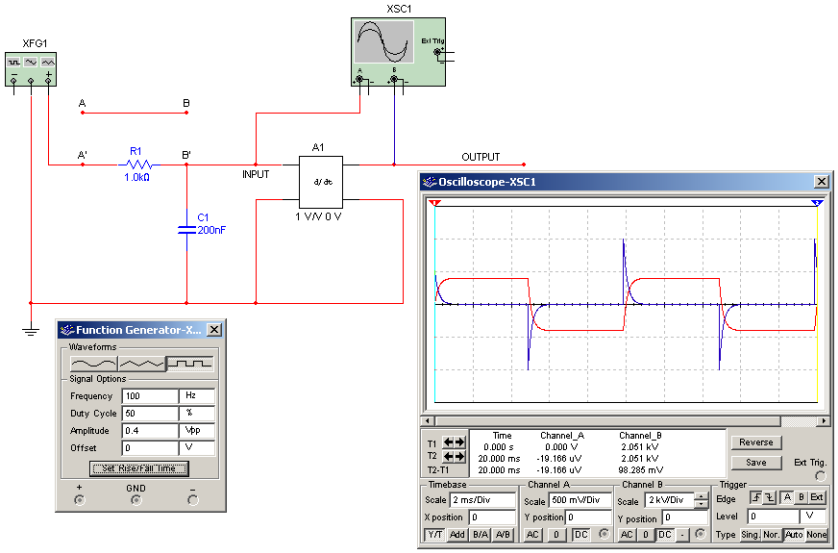
In the example circuit, outputs from the differentiator are limited to +/-5 kilo volts. With the ideal square wave input, the differentiator output will be seen to be +/-5kV.

All real square wave and pulse signals have finite rise times, however small.

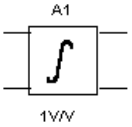
To introduce finite rise and fall times into the input to the differentiator, in order to investigate realistic situations, use an RC network placed in series with the function generator.

***Note*** Since the rise and fall times are fixed, the differentiator output does not change with change of input frequency as for the sine and triangle waveforms.

Changing the RC time constant and comparing differentiator output will illustrate this point.




# 1.33 Voltage Integrator




This component calculates the integral of the input voltage (the transfer function, 1/s) and delivers it to the output. It is used in control systems and analog computing applications.

The true integrator function continuously adds the area under a curve for a specified time interval.

For waveforms that are symmetrical about the zero axis, area above and below the axis is zero and the resulting integrator output is zero.

For waveforms that are not symmetrical about the zero axis, the “areas” will be different. If area above the axis is greater, integrator output will rise. If area is less, integrator output will fall.

### Characteristic Equation

$$V_{out}(t) = K\int_0^t \left(V_i(t) + V_{Ioff}\right)dt + V_{Oic}$$

### Voltage Integrator Parameters and Defaults

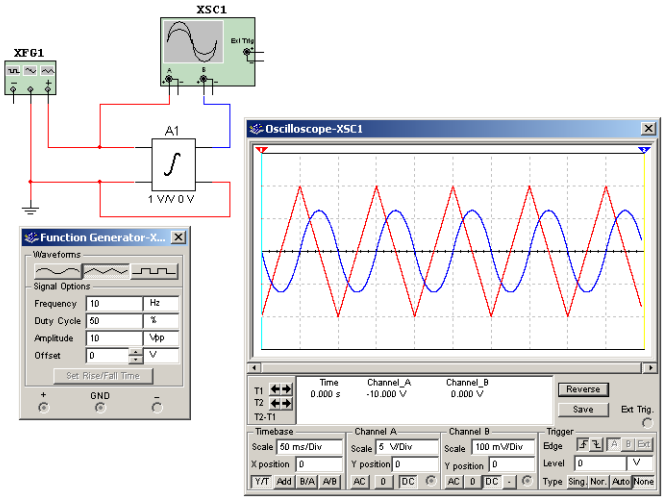
| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| VIoff | Input offset voltage | 0 | V |
| K | Gain | 1 | V/V |
| Vl | Output voltage lower limit | -1e+12 | V |
| Vu | Output voltage upper limit | 1e+12 | V |
| Vs | Upper and lower smoothing range | 1e-06 | V |
| VOic | Output initial conditions | 0 | V |

## 1.33.1 Investigations

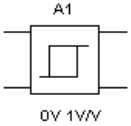
1. In the initial circuit, the input signal is symmetrical (+/- 5V) about the zero axis and the integrator output is zero for sine, square and triangle waveforms.
2. To make the waveforms unsymmetrical about the zero axis use the OFFSET control on the function generator. Setting the OFFSET equal to the AMPLITUDE setting will reference the input to ground (0V).

In this case, the output is always positive. When output is high, “area” is continually added. Output will rise indefinitely.

Changing frequency changes the area. Therefore, in the case of lower frequencies, output rises faster.




# 1.34 Voltage Hysteresis Block




This component is a simple buffer stage that provides hysteresis of the output with respect to the input. ViL and ViH specify the center voltage or current inputs about which the hysteresis effect operates. The output values are limited to VoL and VoH. The hysteresis value, H, is added to ViL and ViH in order to specify the points at which the slope of the hysteresis function would normally change abruptly as the input transitions from low to high values. The slope of the hysteresis function is smoothly varied whenever ISD is set greater than zero.

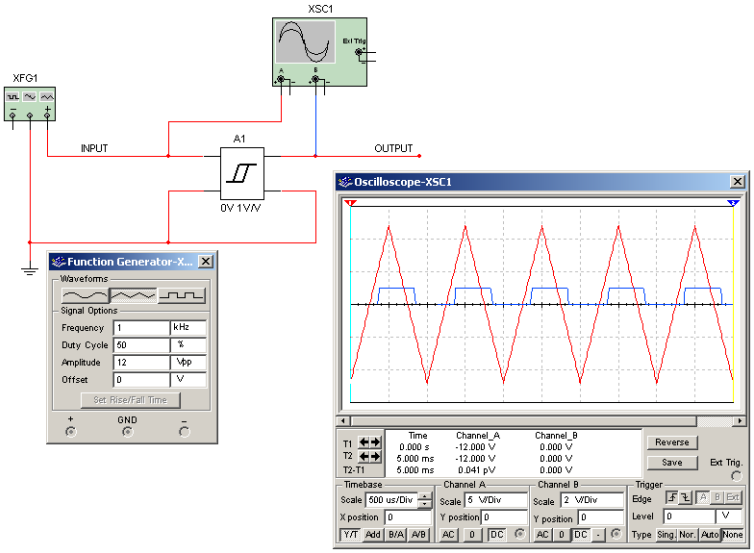
This component can be used to simulate a non-inverting comparator in which the comparison threshold is changed each time the input crosses the threshold in effect at that instant. As the output changes state (high to low or low to high), the threshold voltage is changed internally in such a manner that the input must continue to change until it reaches the new threshold.

In the example circuit shown below, the hysteresis value is set to 5V. This means that the two comparison thresholds at which the output changes are +5V and -5V.

As shown, the input triangle waveform rises from 0V and the output is at its lowest value (0V in this case), as the input crosses +5V (the upper threshold in comparator terms) the output changes to its highest value(+2V in this case). Internally in the hysteresis block the threshold is now changed to -5V, (the lower threshold).

The output continues to rise to a peak and then starts to decrease.

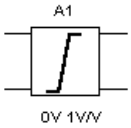
***Note*** The output changes only when the input crosses -5V. Internally, the threshold is changed again to the upper threshold and the process repeats.




## Hysteresis Block Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| ViL | Input low value | 0 | V |
| ViH | Input high value | 1 | V |
| H | Hysteresis | 0.1 | - |
| VoL | Output lower limit | 0 | V |
| VoH | Output upper limit | 1 | V |
| ISD | Input smoothing domain % | 1 | - |

# 1.35 Voltage Limiter



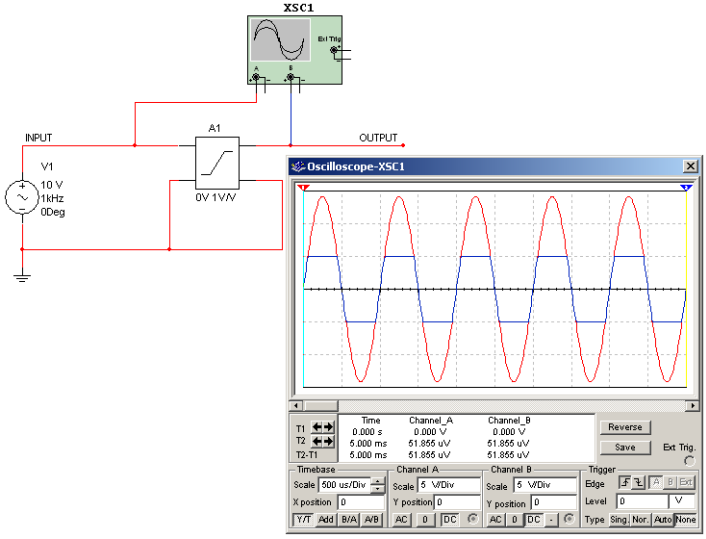

This is a voltage “clipper”. The output voltage excursions are limited, or clipped, at predetermined upper and lower voltage levels while input-signal amplitude varies widely.

In the example shown below, the upper voltage limit is set to +5V and the lower limit is set to - 5 volts. These settings provide symmetrical clipping on the positive and negative peak excursions of the input waveform when these peaks exceed the set limit (clipping) values.

The 10 v RMS (14.14v peak) input is limited at +/-5V.

***Note*** If the input peak voltages are within the set limiting voltages, the input signal is passed through the limiter circuit undistorted.

Unsymmetrical clipping is selected by setting the limit voltages to different values (i.e. +5V and -2V). This technique may be used to produce non-standard waveshapes, starting with sine, triangle sawtooth and other symmetrical waveforms.



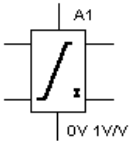
### Characteristic Equation

$$V_{OUT} = K(V_{in} + V_{Ioff}) \text{ for } V_{\min} \le V_{out} \le V_{\max}$$
$$V_{OUT} = V_{\max} \quad \text{for } V_{OUT} > V_{\max}$$
$$V_{OUT} = V_{\min} \quad \text{for } V_{OUT} < V_{\min}$$

### Voltage Limiter Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| VIoff | Input offset voltage | 0 | V |
| K | Gain | 1 | V/V |
| Vl | Output voltage lower limit | 0 | V |
| Vu | Output voltage upper limit | 1 | V |
| Vs | Upper and lower limit smoothing range | 1e-06 | V |

# 1.36 Current Limiter Block




This component models the behavior of an operational amplifier or comparator at a high level of abstraction. All of its pins act as inputs; three of them also act as outputs. The component takes as input a voltage value from the “in” connector. It then applies the offset and gain, and derives from it an equivalent internal voltage, Veq, which it limits to fall between the positive and negative power supply inputs. If Veq is greater than the output voltage seen on the “out” connector, a sourcing current will flow from the output pin. Otherwise, if Veq is less than the output voltage, a sinking current will flow into the output pin.

Depending on the polarity of the current flow, either a sourcing or a sinking resistance (Rsrc or Rsnk) value is applied to govern the output voltage/output current relationship. The chosen resistance will continue to control the output current until it reaches a maximum value

specified by either ISrcL or ISnkL. The latter mimics the current limiting behavior of many operational amplifier output stages.

During operation, the output current is reflected either in the positive or the negative power supply inputs, depending on the polarity of the output current. Thus, realistic power consumption as seen in the supply rails is modeled.

ULSR controls the voltage below positive input power and above negative input power beyond which $V_{eq}$ = k (input voltage + Off) is smoothed. ISrcSR specifies the current below ISrcL at which smoothing begins, and specifies the current increment above zero input current at which positive power begins to transition to zero. ISnkSR serves the same purpose with respect to ISnkL and negative power. VDSR specifies the incremental value above and below ($V_{eq}$ - output voltage) = 0 at which output resistance will be set to Rsrc and Rsnk, respectively. For values of ($V_{eq}$ - output voltage) less than VDSR and greater than -VDSR, output resistance is interpolated smoothly between Rsrc and Rsnk.

The current limiter block is also a representation of an operational amplifier with respect to the sourcing and sinking of current at the output and supply terminals.

If the current being sinked/sourced to the load is less than the rated maximum, as determined from rated maximum sink/source specifications for a particular opamp, operation of the opamp circuit will be as expected.

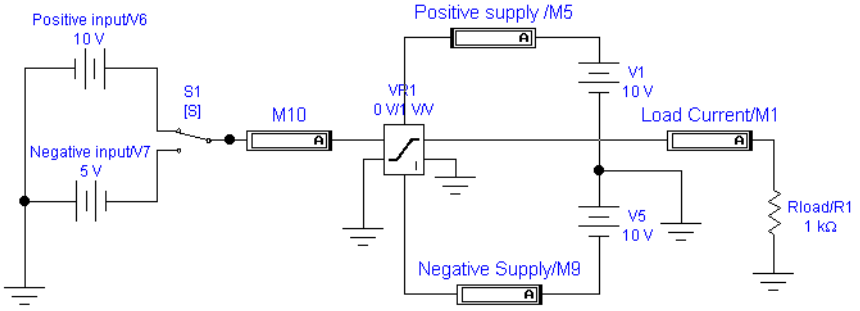
If the current to be sinked/sourced is greater than the rated maximum, as determined by a larger than normal input to the opamp circuit, the current limiter will limit current to the specified safe maximum value, thus protecting the opamp and associated circuitry from damage.

In the example circuit shown below, the sink and source current limits are set to 2 mA and the circuit gain (K) is set to 1. For this case, output current should then be Iload = Vin*K/Rload.

The switch, activated by pressing S, applies either a positive or negative input to the 'op-amp' circuit. These input levels are such that the output current would be in excess of the rated value of 2.0mA. The current limit function limits the source or sink output to 2.0 mA.

If the input levels are reduced to 2V or less, then the output current will be as expected at Vin/Rload.

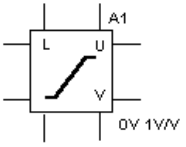
A sine wave input of 1.4v RMS or less will be passed undistorted through the “amplifier” while inputs greater than 1.4 v RMS will show limiting (clipping) at the peaks.




## Current Limiter Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| Off | Input offset | 0 | V |
| k | Gain | 1 | V/V |
| Rsrc | Sourcing resistance | 1 | Ω |
| Rsink | Sinking resistance | 1 | Ω |
| ISrcL | Current sourcing limit | 10 | mA |
| ISnkL | Current sinking limit | 10 | mA |
| ULSR | Upper and lower power supply smoothing range | 1 | $\mu V$ |
| ISrcSR | Sourcing current smoothing range | 1 | nA |
| ISnkSR | Sinking current smoothing range | 1 | nA |
| VDSR | Internal/external voltage delta smoothing range | 1 | νΩ |

# 1.37 Voltage-Controlled Limiter



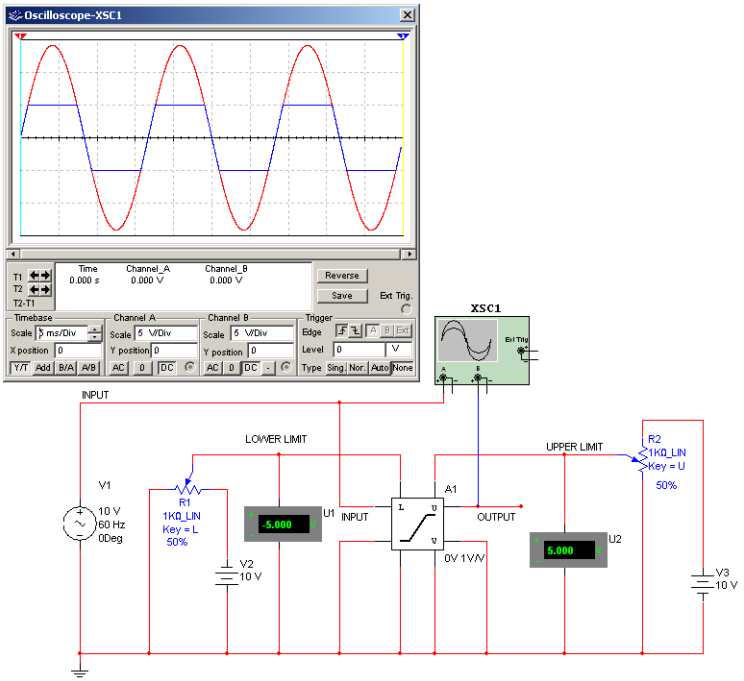

A voltage “clipper”. This component is a single input, single output function. The output is restricted to the range specified by the output lower and upper limits. Output smoothing occurs within the specified range. The voltage-controlled limiter will operate in DC, AC and transient analysis modes.

The component tests the values of the upper and lower limit control inputs to make sure that they are spaced far enough apart to guarantee the existence of a linear range between them. The range is calculated as the difference between (upper limit control input (U) - VoUD - ULSR) and (lower limit control input (L) + VoLD + ULSR) and must be greater than or equal to zero.

The limiting levels may be individually set at fixed values or one or both limiting levels may be controlled by a variable voltage, depending on the desired application.

In the circuit shown below, the upper voltage limit is set by adjusting the potentiometer supplying the Upper terminal on the VCL. The lower voltage limit is set by adjusting the potentiometer supplying the Lower terminal on the VCL. The potentiometers are adjusted by pressing U or SHIFT-U for the upper limit and L or SHIFT-L for the lower limit.

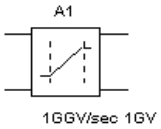
These settings may be adjusted to provide symmetrical or unsymmetrical clipping on the positive and negative peak excursions of the input waveform when these peaks exceed the set limit (clipping) values.




## Voltage-Controlled Limiter Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| ViOff | Input offset | 0 | V |
| k | Gain | 1 | V/V |
| VoUD | Output upper delta | 0 | V |
| VoLD | Output lower delta | 0 | V |
| ULSR | Upper and lower smoothing range | 1 | $\mu V$ |

# 1.38 Voltage Slew Rate Block




This component limits the absolute slope of the output, with respect to time, to some maximum or value. You can accurately model actual slew rate effects of over-driving an amplifier circuit by cascading the amplifier with this component. Maximum rising and falling slope values are expressed in volts per second.

The slew rate block will continue to raise or lower its output until the difference between input and output values is zero. After, it will resume following the input signal unless the slope again exceeds its rise or fall slope limits.

This component provides for introduction of selectable rising and falling slew rates (rise and fall times on a pulse waveform) for analysis of pulse and analog circuits.

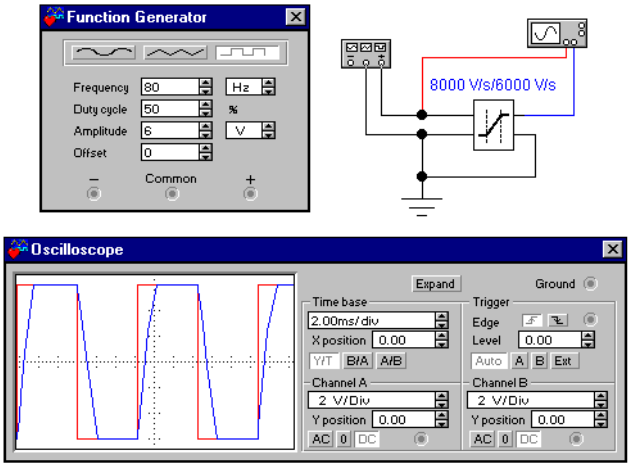
With an ideal pulse or analog input to block the effect of slew rate on a logic circuit or analog amplifier, (discrete component or op-amp) output may be investigated.

In the example shown below, the function generator may be set for either square wave or sine wave output.

A slew rate of 8000V/sec for rising slope and 6000V/sec for falling slope shows as rise and fall time on an ideal 80Hz. square wave input. Signal degradation as a result of slew rate occurs when frequency is increased.

Switching the function generator to sine wave output 60 Hz. does not result in distortion. However, as frequency is increased, slew rate distortion on a sine wave will become evident at 200 Hz. and above. As frequency is increased, the sine wave deteriorates to a triangle shape.

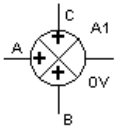
A more serious degradation of output as a result of slew rate occurs when the input frequency is doubled to 200Hz.




### Voltage Slew Rate Block Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| RSMax | Maximum rising slope value | 1 | GV/s |
| FSMax | Maximum falling slope value | 1 | GV/s |

# 1.39 Three-Way Voltage Summer




This component is a math functional block that receives up to three voltage inputs and delivers an output equal to their arithmetic sum. Gain for all three inputs as well as the summed output may be set to match any three input summing application.

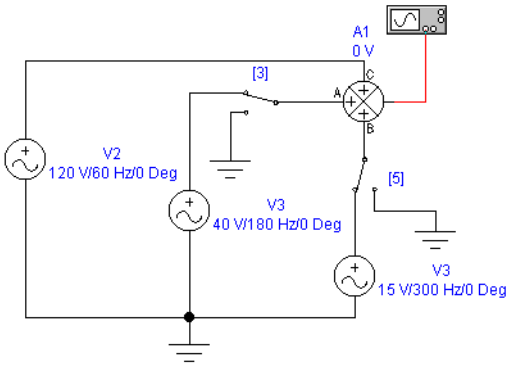
In the example shown below, all gains are set to unity.

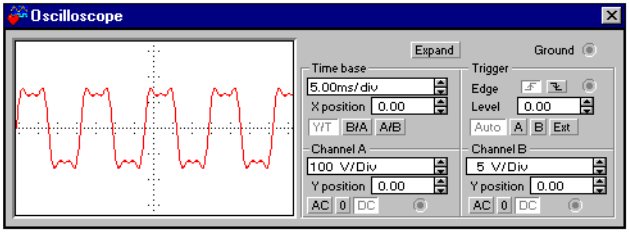
The summer may be used to illustrate the result of adding harmonically related sine wave components which make up a complex waveform (the first three terms in the Fourier expression defining the waveform).

In the example, a fundamental frequency of 60 Hz. and the third and fifth harmonics (in phase) may be progressively added to illustrate the basic makeup of a square wave.

Amplitude and phase of any of the signals may be varied to experiment further.

**Caution** The switches should not be operated while a solution is in progress. This will result in solution error messages. Allow the solution to pause (or pause it by clicking on the solution switch). Operate a switch to add the desired harmonic, and then solve the circuit again.




## Charactistic Equation

$$V_{OUT} = K_{OUT}[K_A(V_A + V_{Aoff}) + K_B(V_B + V_{Boff}) + K_C(V_C + V_{Coff})] + V_{0off}$$

### Summer Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| VAoff | Input A offset voltage | 0 | V |
| VBoff | Input B offset voltage | 0 | V |
| VCoff | Input C offset voltage | 0 | V |
| Ka | Input A gain | 1 | V/V |
| Kb | Input B gain | 1 | V/V |
| Kc | Input C gain | 1 | V/V |
| Kout | Output gain | 1 | V/V |
| VOoff | Output offset voltage | 0 | V |

# 1.40 Three Phase Delta

This component provides a 3 phase power source. The 3 output pins provide 120 degree phase shifted output. The user can define the amplitude, frequency, and delay time. This part is used predominantly in Power applications. The 3 sine wave sources are configured in a delta type connection.

# 1.41 Three Phase Wye

This component provides a 3 phase power source. The user can define the amplitude, frequency, and delay time. The foUrth connection (out the opposite side of the symbol) is used as a Neutral connection. (to ground, or as a return line for unbalanced loads.)

# 1.42 Thermal Noise Source

The Thermal Noise Source uses a Gaussian White Noise model to simulate thermal noise (also known as Johnson noise) in a conductor. It can be placed in series with a resistor to emulate the thermal noise generated by that resistor.

Thermal Noise results from charges bound to thermally vibrating molecules, which produce EMF (electro-motive force) at the open terminals of a conductor.

One disadvantage of using a Gaussian White Noise model for this purpose is that its power would be infinite, however, the model is valid over a limited bandwidth (B) as all EMF fluctuations outside of the defined bandwidth are ignored.

The rms voltage associated with Johnson Noise in a resistor R, at the temperature T (Kelvin) over a bandwidth B (in Hertz) is given by the equation:

Vrms (B) = (4kTRB)^1/2 volts, where k = Boltzmann's Constant = 1.38 e-23 j/d)

The mean power over a bandwidth B is given by the equation:

Power (B) = 4kTRB watts

To set up the Thermal Noise Source, input the required parameters in the **Value** tab of the component's properties dialog box. (Double-click on the placed component to access the dialog box).

# 1.43 TDM Source




TDM Voltage Source




TDM Current Source

The TDM source is used to input National Instruments binary measurement files (`.tdm`) into a Multisim simulation. It is available as both a voltage source and a current source.

➢ To set up the TDM source:

1. Double-click on the TDM source to open its properties dialog box and click the **Value** tab.
2. In the **File** area:
   - **Filename** — click on the button to the right of this field and navigate to the desired `.tdm` file. When the **Select Trace** dialog box appears, enter the desired **Group**, **Channel X** and **Channel Y** data, or click **OK** to accept the default settings.

***Note*** If you do not specify a filename, the component behaves like an open circuit. An error message does not display in this case.

- **Preview Data** — select to view the file's contents in the **Value** tab.
- **Reload File** — click to reload the file when the `.tdm` file has been edited and you wish to reflect the changes in the TDM Source.
- **Repeat** — enable to continuously run the file during simulation. If this checkbox is not enabled, output from the source will cease once the final data pair has been read.

3. In the **Channel** area:
   - **Select Channel** — displays the **Select Trace** dialog box where you can edit the **Group**, **Channel X** and **Channel Y** settings.
   - **Channel Group** — displays the selected group.
   - **Channel X** — displays the selected x channel.
   - **Channel Y** — displays the selected y channel.
4. Click **OK** to close the source's properties dialog.

### Binary Measurement Files

When data is saved as a binary measurement file, two files are created; a header file (`.tdm`) and a binary file (`.tdx`). For this source to function both of these files, with the same base name (e.g., `sample.tdm` and `sample.tdx`) must be present .

***Note*** Implicit channels are not supported. By default, the first channel will be the x-axis data.

# 1.44 LVM Source




LVM Voltage Source




LVM Current Source

The LVM source is used to input National Instruments text-based measurement files (`.lvm`) into a Multisim simulation. It is available as both a voltage source and a current source.

➢ To set up the LVM source:

1. Double-click on the LVM source to open its properties dialog box and click the **Value** tab.
2. In the **File** area:
   - **Filename** — click on the button to the right of this field and navigate to the desired `.lvm` file. When the **Select Trace** dialog box appears, enter the desired **Section** and

**Channel** data, or click **OK** to accept the default settings.

- **Preview Data** — select to view the file's contents in the **Value** tab.
- **Reload File** — click to reload the file when the `.lvm` file has been edited and you wish to reflect the changes in the LVM Source.
- **Repeat** — enable to continuously run the file during simulation. If this checkbox is not enabled, output from the source will cease once the final data pair has been read.

3. In the **Channel** area:
   - **Select Channel** — displays the **Select Trace** dialog box where you can edit the **Section** and **Channel** settings.
   - **Section** — displays the selected section.
   - **Channel** — displays the selected channel.
4. Click **OK** to close the source's properties dialog.

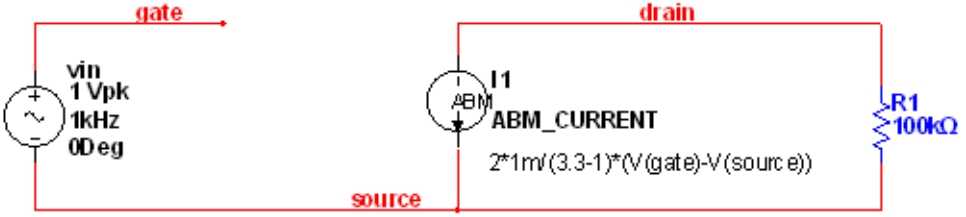
# 1.45 ABM Sources

ABM (analog behavioral model) sources use mathematical and conditional expressions to set their output voltage or current. They may contain mathematical and conditional expressions that consist of circuit voltages, currents, time and other simulation parameters.

➢ To enter an expression in a current or voltage ABM source:

1. Double-click on the placed component ABM source and click the **Value** tab.
2. Enter the expression in the **Current Value** (in current sources) or **Voltage Value** (in voltage sources) field.

The example circuit below is an ABM current source with value `2*0.001/(3.3-1)*(V(gate)-V(source))`:




Expressions may use node voltages relative to ground using the syntax `V(<net name>)`, where `<net name>` is the name of a net. Alternatively, expressions may use differential node voltages using the syntax `V(<net name1>, <net name2>)`, where the expression evaluates to the difference between nets `<net name1>` and `<net name2>`.

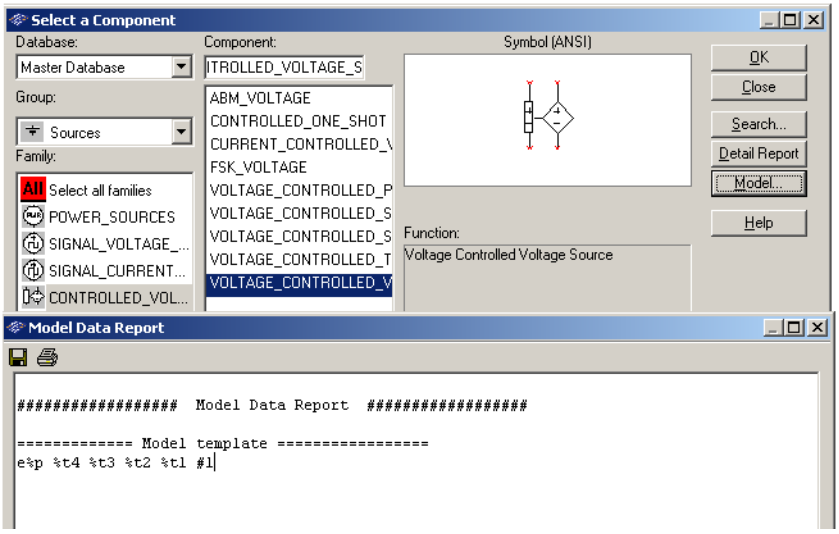
Expressions may use reference branch currents through voltage source elements using the syntax `I(<source_type><refdes>)`, where `<source type>` is a single letter specifying a the type of SPICE primitive source and `<refdes>` is the schematic reference designator of the voltage source.

Multisim supports referencing current through four types of SPICE primitive voltage sources:

- Independent source ("V" source)
- Voltage-Controlled Voltage-Source ("E" source)
- Current-Controlled Voltage-Source ("H" source)
- ABM source ("B" source).

➢ To easily determine the referenced source type:

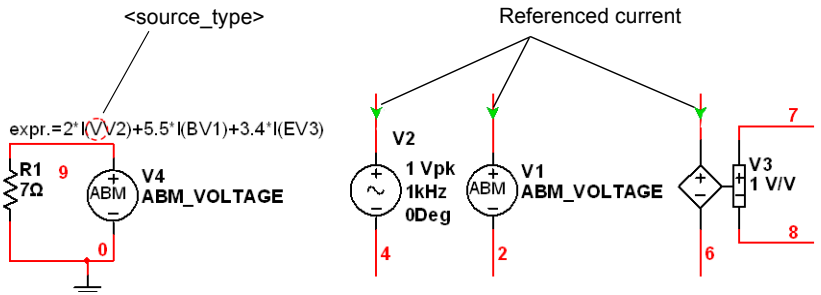
1. Click the **Model** button in the **Select a Component** dialog. The component's SPICE template displays as in the example below.




The first letter of the model template must be one of `V,E,H,` or `B`. This is the `<source_type>`. If the first letter is any but `V,E,H,` or `B` (e.g., templates using `SUBCKTs`), you may not reference current passing through this component.

In the case of a circuit branch in which there is no voltage source component, or there is a voltage source component which may not be referenced, break the branch and insert a 0-volt voltage source that has valid template for referencing (e.g., the DC_POWER component).

The example below is an ABM voltage source whose expression references current through three different types of voltage source components.




***Note*** Positive current polarity is taken from the positive node to the negative node of the voltage source.

Multisim supports a rich set of operators and functions which can be used in expressions. For details, refer to "Analog Behavioral Modeling and Controlled Source Syntax" in your *Multisim User Guide* or helpfile.

# 1.46 Bipolar Sources

The bipolar current and voltage sources provide a pulsed current or voltage output.

➢ To change the output of a bipolar source:

1. Double-click on the source to open its properties dialog box and click the **Value** tab.
2. Change the following as desired:
   - **Positive Pulse** <**Current** or **Voltage**> — depending on the source type, this is either the value of the positive current or negative voltage pulse
   - **Negative Pulse** <**Current** or **Voltage**> — depending on the source type, this is either the value of the negative current or negative voltage pulse
   - <**Current** or **Voltage**> **Offset** — depending on the source type, this is either the value of the current or the voltage offset
   - **Duty Cycle/Pulse Duration Time** — enter either value and the other changes automatically
   - **Frequency(F)/Period** — enter either value and the other changes automatically
   - **Rise Time**
   - **Fall Time**
   - **Dead Time/Dead Time Rate** — enter either value and the other changes automatically
   - Effective Duty Cyle — read-only value that changes as you edit **Duty Cycle/Pulse Duration Time** or **Dead Time/Dead Time Rate**.
3. Click **OK** to accept the changes and close the dialog.

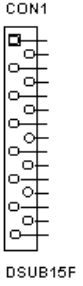
# 1.47 GAIN_2_PIN

This device is a voltage-controlled voltage source.

- To edit this device's parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Change the **Voltage Gain** as desired.

# Chapter 2
# Basic Components

## 2.1 Connectors




Connectors are mechanical devices used to provide a method of inputting and outputting signals to a design. They do not affect the simulation of the circuit but are included in the circuit for the design of the PCB.

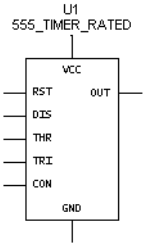
## 2.2 Rated Virtual Components

This component family contains a number of virtual components that can be rated to "blow" if pre-set tolerance(s) are exceeded when the circuit is simulated. These tolerances are set in the **Values** tab of each component's properties window.

***Tip*** "Rated" values in a component's **Value** tab define behavior and design. "Maximum" values impose limits that, when exceeded, cause the component to "blow".

The rated virtual components are found in the **Basic** group in the **Rated Virtual** family.

## 2.2.1 Rated 555 Timer




The 555 timer is an IC chip that is commonly used as an astable multivibrator, a monostable multivibrator or a voltage-controlled oscillator. The 555 timer consists basically of two comparators, a resistive voltage divider, a flip-flop and a discharge transistor. It is a two-state device whose output voltage level can be either high or low. The state of the output can be controlled by proper input signals and time-delay elements connected externally to the 555 timer.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of the 555 timer.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Maximum Supply Voltage** — the maximum supply voltage allowed. If this is exceeded during simulation, the timer's VCC pin blows.
   - **Maximum Output Current** — the maximum output current allowed. If this is exceeded during simulation, the timer's OUT pin blows.
3. Click **OK**.

## 2.2.2 Rated BJTs



A bipolar junction transistor, or BJT, is a current-based valve used for controlling electronic current. BJTs are operated in three different modes, depending on which element is common to input and output: common base, common emitter or common collector. The three modes have different input and output impedances and different current gains, offering individual advantages to a designer.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of BJTs.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Maximum Collector-Emitter Voltage** — the maximum collector-emitter voltage allowed. If this value is exceeded during simulation, the BJT blows.
   - **Maximum Collector-Base Voltage** — the maximum collector-base voltage allowed. If this value is exceeded during simulation, the BJT blows.
   - **Maximum Emitter-Base Voltage** — the maximum emitter-base voltage allowed. If this value is exceeded during simulation, the BJT blows.
   - **Maximum Collector Current** — the maximum collector current allowed. If this value is exceeded during simulation, the BJT blows.
   - **Saturation Current** — the maximum saturation current allowed. If this value is exceeded during simulation, the BJT blows.
   - **Maximum Forward Beta** — the maximum forward beta allowed. If this value is exceeded during simulation, the BJT blows.
3. Click **OK**.

## 2.2.3 Rated Capacitors




A capacitor stores electrical energy in the form of an electrostatic field. Capacitors are widely used to filter or remove AC signals from a variety of circuits. In a DC circuit, they can be used to block the flow of direct current while allowing AC signals to pass.

A capacitor's capacity to store energy is called its capacitance, *C,* which is measured in farads.

The variable capacitor is simulated as an open circuit with a current across the capacitor forced to zero by a large impedance value.

The polarized capacitor must be connected with the right polarity. Otherwise, an error message will appear.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of capacitors.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Capacitance** — set the capacitance as desired.
   - **Voltage Rating (Pk)** — the maximum peak voltage across the capacitor allowed. If this value is exceeded during simulation, the capacitor blows.
   - **Initial Conditions** — the initial charge across the capacitor, before simulation begins.
3. Click **OK**.

## 2.2.4 Rated Diodes



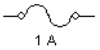

Diodes allow current to flow in only one direction and can therefore be used as simple solid-state switches in AC circuits, being either open (not conducting) or closed (conducting). Terminal A is called the anode and terminal K is called the cathode.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of diodes.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Reverse Breakdown Voltage** — set as desired.
   - **Current at Breakdown Voltage** — set as desired.
   - **Saturation Current** — the maximum current through the capacitor allowed. If this value is exceeded during simulation, the diode blows.
   - **Transit Time (sec)** — used to model charge storage effects - pertains to the electrons lifetime, alternately the hole lifetime at the p-n junction.
3. Click **OK**.

## 2.2.5 Rated Fuses




This is a resistive component that protects against power surges and current overloads.

A fuse will blow (open) if the current in the circuit goes above $I_{max}$, the maximum current rating.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of fuses.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Maximum Current (Imax)** — the maximum current allowed through the fuse. If this value is exceeded during simulation, the fuse blows.
3. Click **OK**.

## 2.2.6 Rated Inductors




An inductor stores energy in an electromagnetic field created by changes in current through it. Its ability to oppose a change in current flow is called inductance, *L,* and is measured in Henrys.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of inductors.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Inductance** — the coil's inductance. Set as desired.
   - **Coil Resistance** — set as desired.
   - **Current Rating (Pk)** — the maximum peak current allowed through the inductor. If this value is exceeded during simulation, the inductor blows.
   - **Initial Conditions** — the initial current through the inductor, before simulation begins.
3. Click **OK**.

## 2.2.7 Rated LEDs



This diode emits visible light when forward current through it, $I_{d,}$ exceeds the turn-on current, $I_{on}$. The electrical model of the LED is the same as the diode model.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of LEDs.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.

2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **On Current (Ion)** — the current required to switch the LED on.
   - **Reverse Breakdown Voltage** — set as desired.
   - **Maximum Rated Power (Watts)** — the maximum power dissipation across the LED allowed. If this value is exceeded during simulation, the inductor blows.
3. Click **OK**.

## 2.2.8 Rated DC Motor



The component is a universal model of an ideal DC motor which can be used to model the behavior of a DC motor excited in parallel, in series or separately.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of DC motors.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Rated Armature Voltage (Van)** — set as desired.
   - **Maximum Armature Voltage** — the maximum voltage across the armature allowed. If this value is exceeded during simulation, the motor blows.
   - **Rated Armature Current (Ian)** — set as desired.
   - **Maximum Armature Current** — the maximum current through the armature allowed. If this value is exceeded during simulation, the motor blows.
   - **Rated Field Voltage (Vfn)** — set as desired.
   - **Maximum Field Voltage** — the maximum field voltage allowed. If this value is exceeded during simulation, the motor blows.
   - **Armature Resistance (Ra)** — set as desired.
   - **Armature Inductance (La)** — set as desired.
   - **Field Resistance (Rf)** — set as desired.
   - **Field Inductance (Lf)** — set as desired.

***Tip*** To view the following fields, click in a blank space in the **Value** tab and drag the mouse upward.

- **Shaft Friction (Bf)** — set as desired.
- **Rotational Inertia (J)** — set as desired.
- **Rated Rotational Speed (NN)** — set as desired.
- **Load Torque (Tl)** — set as desired.

3. Click **OK**.

## 2.2.9 Rated Relay



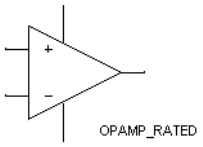

The magnetic relay is a coil with a specified inductance that causes a contact to open or close when a specified current (Ion) charges it.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of relays.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Coil Inductance** — set as desired.
   - **Coil Resistance** — set as desired.
   - **On Current (Ion)** — set as desired.
   - **Off Current (Ioff)** — set as desired .
   - **Maximum Rated Voltage** — the maximum voltage allowed. If this value is exceeded during simulation, the relay blows.
   - **Maximum Rated Current** — the maximum current allowed. If this value is exceeded during simulation, the relay blows.
3. Click **OK**.

# 2.2.10 Rated Opamp




An ideal operational amplifier (Opamp) is an amplifier with infinite gain, infinite input impedance and zero output impedance. With the application of negative feedback, Opamps can be used to implement functions such as addition, subtraction, differentiation, integration, averaging and amplification.

An opamp can have a single input and single output, a differential input and single output, or a differential input and differential output.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of opamps.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Maximum Supply Voltage (+/-)** — the maximum voltage (+/) allowed. If this value is exceeded during simulation, the opamp blows.
   - **Maximum Input Voltage (+/-)** — the maximum input voltage (+/) allowed. If this value is exceeded during simulation, the opamp blows.
   - **Maximum Differential Input Voltage** — the maximum differential input voltage allowed. If this value is exceeded during simulation, the opamp blows.
   - **Maximum Sink/Source Output Current** — If this value is exceeded during simulation, the opamp blows.
3. Click **OK**.

## 2.2.11 Rated Photodiode




The photodiode emits a source of infrared light which is detected by the phototransistor. These devices are intended to be used in pairs.

You must specify a light channel in each of these paired parts (photodiode and phototransistor). This is done in the **Value** tab of the component's properties screen. Each diode must have a different value for its light channel, however, the phototransistor can share the same value with several other phototransistors.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Light Channel (Integer)** — set to match the light channel for the corresponding phototransistor(s).
   - **On Current (Ion)** — set as desired.
   - **Reverse Breakdown Voltage** — set as desired.
   - **Maximum Rated Power (Watts)** — If this value is exceeded during simulation, the photodiode blows.
3. Click **OK**.

## 2.2.12 Rated Phototransistor



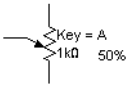

The photodiode emits a source of infrared light which is detected by the phototransistor. These devices are are intended to be used in pairs.

You must specify a light channel in each of these paired parts (photodiode and phototransistor). This is done in the **Value** tab of the component's properties screen. Each diode must have a different value for its light channel, however, the phototransistor can share the same value with several other phototransistors.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Light Channel (Integer)** — set to match the light channel for the corresponding photodiode.
   - **Maximum Collector-Emitter Voltage** — If this value is exceeded during simulation, the phototransistor blows.
   - **Maximum Collector Current** — If this value is exceeded during simulation, the phototransistor blows.
3. Click **OK**.

## 2.2.13 Rated Potentiometer




This component acts much like a tapped/split resistor, except that you can adjust its resistance.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of potentiometers.

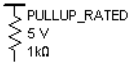
➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Key —** enter the key that will increase the resistance by the amount set in the **Increment** field.
   - **Increment —** enter the amount by which the resistance will increase when the key set in the **Key** field is pressed.
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.

- **Resistance** — the maximum resistance of the potentiometer.
- **Maximum Rated Power (Watts)** — If this value is exceeded during simulation, the potentiometer blows.

3. Click **OK**.

## 2.2.14 Rated Pullup




This component is used to raise the voltage of a circuit to which it is connected. One end is connected to Vcc. The other end is connected to a point in a logic circuit that needs to be raised to a voltage level closer to Vcc.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Voltage (V)** — set as desired.
   - **Resistance** — set as desired.
   - **Maximum Rated Power (Watts)** — If this value is exceeded during simulation, the pullup blows.
3. Click **OK**.

## 2.2.15 Rated Resistor



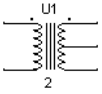

Resistors come in a variety of sizes, related to the power they can safely dissipate.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of resistors.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Resistance** — set as desired.
   - **Maximum Rated Power (Watts)** — If this value is exceeded during simulation, the resistor blows.
   - **Temperature** — set as desired.
   - **Temperature Coefficient 1** — set as desired.
   - **Temperature Coefficient 2** — set as desired.
   - **Nominal Temperature** — set as desired.
3. Click **OK**.

## 2.2.16 Rated Transformers




The transformer is one of the most common and useful applications of inductance. It can step up or step down an input primary voltage (V1) to a secondary voltage (V2). The relationship is given by V1/V2 = n, where n is the ratio of the primary turns to the secondary turns.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of transformers.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Maximum Primary Voltage** — If this value is exceeded during simulation, the resistor blows.
   - **Maximum Primary Current** — If this value is exceeded during simulation, the resistor blows.
   - **Maximum Secondary 1 Voltage** — If this value is exceeded during simulation, the

resistor blows.

- **Maximum Secondary 1 Current** — If this value is exceeded during simulation, the resistor blows.
- **Maximum Secondary 2 Voltage** — If this value is exceeded during simulation, the resistor blows.
- **Maximum Secondary 2 Current** — If this value is exceeded during simulation, the resistor blows.
- **Maximum Output Power (kVA)** — If this value is exceeded during simulation, the resistor blows.
- **Primary-to-Secondary Turns Ratio** — set as desired.
- **Leakage Inductance (Le)** — set as desired.
- **Magnetizing Inductance (Lm)** — set as desired.

***Tip*** To view the following fields, click in a blank space in the **Value** tab and drag the mouse upward.

- **Primary Winding Resistance** — set as desired.
- **Secondary Winding Resistance** — set as desired.

3. Click **OK**.

# 2.2.17 Rated Variable Capacitor




This component acts much like a regular capacitor, except that you can, with a single keystroke, adjust its capacitance.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of capacitors.

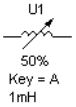
➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Key —** enter the key that will increase the capacitance by the amount set in the **Increment** field.
   - **Increment —** enter the amount by which the capacitance will increase when the key set in the **Key** field is pressed (instead of pressing the key, you can hover your cursor over the variable capacitor and click the button that pops up).
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the

symbol blowing. This is not a real-time value.
- **Capacitance** — the maximum capacitance of the variable capacitor.
- **Initial Conditions** — the charge across the capacitor that is present before simulation starts.
- **Voltage Rating (Pk)** — If this value is exceeded during simulation, the capacitor blows.

3. Click **OK**.

## 2.2.18 Rated Variable Inductor




This component acts much like a regular inductor, except that you can, with a single keystroke, adjust its inductance.

***Note*** Refer to the *Component Reference Guide* for a more detailed discussion of inductors.

➢ To adjust the component's tolerances:

1. Double-click on the placed component and click the **Value** tab.
2. Change the following values as desired:
   - **Key —** enter the key that will increase the inductance by the amount set in the **Increment** field.
   - **Increment —** enter the amount by which the inductance will increase when the key set in the **Key** field is pressed (instead of pressing the key, you can hover your cursor over the variable inductor and click the button that pops up).
   - **Animation Delay Factor** — increase this number to slow the speed of animation of the symbol blowing. This is not a real-time value.
   - **Inductance** — the maximum inductance of the variable inductor.
   - **Coil Resistance** — set as desired.
   - **Initial Conditions** — the current through the inductor that is present before simulation starts.
   - **Current Rating (Pk)** — If this value is exceeded during simulation, the inductor blows.
3. Click **OK**.

## 2.2.19 Rated Virtual Components Toolbar

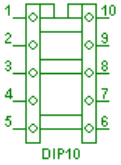



Some of the more commonly-used rated virtual components can be placed using the **Rated Virtual Components** toolbar.

- To display the **Rated Virtual Components** toolbar, click the **Show Rated Family** button in the **Virtual** toolbar (refer to the *Multisim User Guide* for **Virtual** toolbar information).

  The buttons (from left to right) in the **Rated Virtual Components** toolbar place the following virtual components: NPN transistor; PNP transistor; Capacitor; Diode; Inductor; Motor; normally closed relay; normally open relay; combination relay; resistor.

# 2.3 Sockets




Sockets are mechanical devices that are used to connect devices onto a PCB. They do not affect the simulation of the circuit but are included for the design of the PCB.

# 2.4 Switch




Switches are interactive components that can be closed or opened (turned on or off) by pressing a key on the keyboard, or by using the mouse.

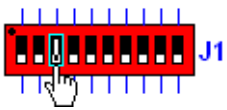
- To specify the key that controls the switch:
  1. Double-click on the switch and select its **Value** tab.
  2. Select the key in the **Key for Switch** drop-down list and click **OK**.
- To toggle the switch on or off using the keyboard, press the identified key.
- To toggle the switch on or off using the mouse, hover the cursor over the switch's arm and click when the arm takes on a thickened appearance.

### Non-interactive Switches

A small number of switches, for example, time delayed switches, current controlled switches and voltage controlled switches are not interactive components. For these components, the contents of the **Value** tab will be different than those described above, and will vary depending on the selected component.

Change the settings for these devices in the usual manner; double-click on the component, select the **Value** tab, and enter the desired parameters.

## 2.4.1 Switch Packs




DIP switch packs are available in footprints that contain from 2 to 10 switches. These devices are interactive components that can be closed or opened (turned on or off) by pressing a key on the keyboard, or by using the mouse. The black circle on the switch indicates the ON position for switch number 1 in the pack.

You can set a different activation key for each switch in the pack.

- To set switches' activation keys:
  1. Double-click on the DIP switch pack to display its properties dialog box and click on the **Value** tab.
  2. Enter the desired key for each switch in its corresponding field (**Switch 1 Key**, **Switch 2 Key**, etc.) and click **OK**.
- To toggle a specific switch on or off using the keyboard, press the identified key.
- To toggle a specific switch on or off using the mouse, hover the cursor over the desired switch and click when the switch is highlighted by a rectangle and cursor changes to a hand symbol.

***Note*** Unused switches in a switch pack should be left in the OFF position for simulation. For a discussion of interactive simulation, refer to the *Multisim User Guide*.

# 2.5 SBREAK

This device is a voltage-controlled switch.

➢ To change the component's parameters:

1. Double-click on the placed component and select the **Value** tab.
2. Change the following as desired:
   - **On-state Voltage (VON)** — voltage at which the switch turns on.
   - **Off-state Voltage (VOFF)** — voltage at which the switch turns off.
   - **On-state Resistance (RON)** — resistance of the device during its on-state.
   - **Off-state Resistance (ROF)** — resistance of the device during its off-state.
3. Click **OK** to save to close the dialog box.

# 2.6 Resistor




Resistors come in a variety of sizes, depending on the power they can safely dissipate. A resistor's resistance, R, is measured in ohms. Color-coded stripes on a real-world resistor specify its resistance and tolerance. Larger resistors have this information printed on them.

Any electrical wire has resistance, depending on its material, diameter and length. Wires that must conduct very heavy currents (for example, ground wires on lightning rods) have large diameters to reduce resistance.

The power dissipated by a resistive circuit carrying electric current is in the form of heat. Circuits dissipating excessive energy will literally burn up. Practical circuits must take power capacity into account.

In Multisim, the Resistance, R, of a resistor instance is calculated using the following equation:

R = Ro * { 1 + TC1*(T - To) + TC2*[(T-To)^2] }

where:

R = The resistance of the resistor

Ro = The resistance of the resistor at temperature To

To = Nominal temperature = 27 degrees C [CONSTANT]

TC1 = First order temperature coefficient

TC2 = Second order temperature coefficient

T = Temperature of the resistor

## 2.6.1 About Resistance

Ohm's law states that current flow depends on circuit resistance:

$I = E/R$

Circuit resistance can be calculated from the current flow and the voltage:

$R = E/I$

Circuit resistance can be increased by connecting resistors in series:

$R = R1 + R2 + ... + Rn$

Circuit resistance can be reduced by placing one resistor in parallel with another.

## 2.6.2 Characteristic Equation

The current through the resistor uses the model:

$$i = \frac{V_1 - V_2}{R}$$

where:

i = current

$V_1$ = voltage at node 1

$V_2$ = voltage at node 2

R = resistance

## 2.6.3 Changing a Placed Resistor's Value

- To change the value, and other parameters of a placed resistor:
  1. Double-click on the resistor and select the **Value** tab.
  2. Select the desired resistance from the **Resistance(R)** list. If it is not there, type the value you want.
  3. Select the desired tolerance from the **Tolerance** list, or type in a value.

4. Optionally, enter information in the **Component Type** (for example, carbon film) and **Hyperlink** fields.
5. Optionally, enable the **Additional SPICE Simulation Parameters** fields described below:
   - **Temperature (TEMP)** — the device's operating temperature.
   - **Temperature Coefficient (TC1)** — first order temperature coefficient.
   - **Temperature Coefficient (TC2)** — second order temperature coefficient.
   - **Nominal Temperature (TNOM)** — the normal temperature at which model parameters are measured and calculated.
6. Optionally, change the **Layout Settings** as described below:
   - **Edit Footprint** button — click to display the **Edit Footprint** dialog box where you can select a new **Footprint** and **Manufacturer**.

***Note*** For information on placing resistors, and information on how to edit footprints, refer to the *Multisim User Guide* or the Multisim helpfile.

# 2.7 Capacitor




A capacitor stores electrical energy in the form of an electrostatic field. Capacitors are widely used to filter or remove AC signals from a variety of circuits. In a DC circuit, they can be used to block the flow of direct current while allowing AC signals to pass.

A capacitor's capacity to store energy is called its capacitance, *C,* which is measured in farads.

Capacitors in an AC circuit behave as "short circuits" to AC signals. They are widely used to filter or remove AC signals from a variety of circuits — AC ripple in DC power supplies, AC noise from computer circuits, etc.

Capacitors prevent the flow of direct current in a DC circuit. They can be used to block the flow of DC, while allowing AC signals to pass. Using capacitors to couple one circuit to another is a common practice.

Capacitors take a predictable time to charge and discharge and can be used in a variety of time-delay circuits. They are similar to inductors and are often used with them for this purpose.

## 2.7.1 Characteristic Equation

The current through the capacitor is equal to *C* multiplied by the rate of change in voltage across the capacitor, that is:

$$i = C\frac{dv}{dt}$$

## 2.7.2 DC Model

In the DC model, the capacitor is represented by an open circuit.

## 2.7.3 Time-Domain Model

$R_{cn}$ is an equivalent resistance and $i_{cn}$ is an equivalent current source. The expression for the $R_{cn}$ and $i_{cn}$ depends on the numerical integration method used.

For trapezoid method:

$$R_{cn} = \frac{h}{2C}$$

$$i_{cn} = \frac{2C}{h}V_n + i_n$$

For the first-order Gear method Backward Euler:

$$R_{cn} = \frac{h}{C}$$

$$i_{cn} = \frac{C}{h}V_n$$

where:

$V_{n+1}$ = present unknown voltage across the capacitor

$i_{n+1}$ = present unknown current through the capacitor

$V_{n,\ i}$n = previous solution values

h = time step

n = time interval

These expressions are derived by applying appropriate numerical integration to the characteristic equation of the capacitor.

## 2.7.4 AC Frequency Model

For the small-signal analysis, the capacitor is modeled by an impedance whose imaginary component is equal to:

$$\frac{1}{2\pi fC}$$

where:

f = frequency of operation

C = capacitance value

## 2.7.5 Changing a Placed Capacitor's Value

- To change the value, and other parameters of a placed capacitor:
  1. Double-click on the capacitor and select the **Value** tab.
  2. Select the desired capacitance from the **Capacitance(C)** list. If it is not there, type the value you want.
  3. Select the desired tolerance from the **Tolerance** list, or type in a value.
  4. Optionally, enter information in the **Component Type** (for example, ceramic) and **Hyperlink** fields.
  5. Optionally, enable the **Additional SPICE Simulation Parameters** field described below:
     - **Initial Conditions** checkbox — enable and then enter an initial voltage charge for the capacitor.
  6. Optionally, change the **Layout Settings** as described below:
     - **Edit Footprint** button — click to display the **Edit Footprint** dialog box where you can select a new **Footprint** and **Manufacturer**.

***Note*** For information on placing capacitors, and information on how to edit footprints, refer to the *Multisim User Guide* or the Multisim helpfile.

# 2.8 Inductor




An inductor stores energy in an electromagnetic field created by changes in current through it. Its ability to oppose a change in current flow is called inductance, *L,* and is measured in Henrys.

An inductor is a coil of wire of one “turn” or more. It reacts to being placed in a changing magnetic field by developing an “induced” voltage across the turns of the inductance, and will provide current to a load across the inductance. Voltages can be very large.

Inductors, like capacitors, store energy in magnetic fields. Their “charge” and “discharge” times make them useful in time-delay circuits.

## 2.8.1 Characteristic Equation

The voltage across the inductor is equal to the inductance, *L,* multiplied by the change in current through the inductor, that is:

$$v = L\frac{di}{dt}$$

## 2.8.2 DC Model

In the DC model, the inductor is represented by a short circuit.

## 2.8.3 Time-Domain Model

$R_{Ln}$ is an equivalent resistance and $i_{Ln}$ is an equivalent current source. The expression for the $R_{Ln}$ and $i_{Ln}$ depends on the numerical integration method used.

For trapezoid method:

$$R_{Ln} = \frac{2L}{h}$$

$$i_{Ln} = \frac{h}{2L} V_n + i_n$$

For Gear method (first order):

$$R_{Ln} = \frac{L}{h}$$

$$i_{Ln} = \frac{h}{L} V_n$$

where:

$V_{n+1}$ = present unknown voltage across the inductor

$i_{n+1}$ = present unknown current through the inductor

$V_{n,}$ $i_n$ = previous solution values

h = time step

n = time interval

These expressions are derived by applying appropriate numerical integration to the characteristic equation of the inductor.

## 2.8.4 AC Frequency Model

For the small-signal analysis, the inductor is modeled by an impedance with its imaginary component equal to $2\pi fL$,

where:

f = frequency of operation of the circuit

L = inductance value

### 2.8.5 Changing a Placed Inductor's Value

➢ To change the value, and other parameters of a placed inductor:

1. Double-click on the inductor and select the **Value** tab.
2. Select the desired inductance from the **Inductance(L)** list. If it is not there, type the value you want.
3. Select the desired tolerance from the **Tolerance** list, or type in a value.
4. Optionally, enter information in the **Component Type** (for example, coil) and **Hyperlink** fields.
5. Optionally, enable the **Additional SPICE Simulation Parameters** field described below:
   - **Initial Conditions** checkbox — enable and then enter an initial current for the inductor.
6. Optionally, change the **Layout Settings** as described below:
   - **Edit Footprint** button — click to display the **Edit Footprint** dialog box where you can select a new **Footprint** and **Manufacturer**.

***Note*** For information on placing inductors, and information on how to edit footprints, refer to the *Multisim User Guide* or the Multisim helpfile.

## 2.9 Advanced Inductor

➢ To change the parameters of an advanced inductor:

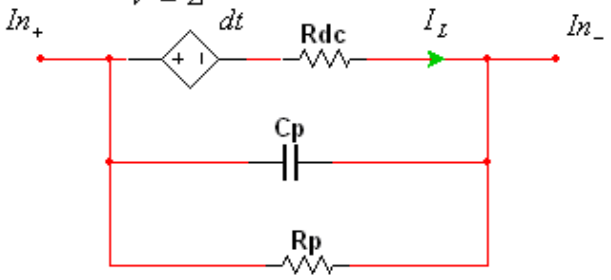
1. Double-click on the placed inductor and select the **Value** tab.
2. Change the parameters listed below as desired:
   - **Nominal Inductance (Lo)** — inductance at low frequency/current.
   - **Inductor Self Resonant Frequency (fo)** — frequency at which the impedance. magnitudes of the nominal inductor and the parasitic capacitor are equal.
   - **Inductor Series Resistance (Rdc)** — resistance of the inductor winding.
   - **Inductor Quality Factor (Q)** — quality factor of the parallel RLC combination.
   - **Inductor Rated Current(Idc)** — current at which the nominal inductance reduces to 90%.
3. Click **OK**.

## Advanced Inductor Model Overview

The advanced inductor model includes both non-ideal AC and DC effects. The simplified subcircuit for the inductor has the following model:

$$L = Lo(1 - \frac{I_L^2}{10 I_{dc}^2})$$

$$V = L\frac{dI_L}{dt}$$




The actual inductor model includes a dependent voltage source that is proportional to the derivative of the current, $I_L$. See “Advanced Inductor Model Implementation” on page 2-28 for a more detailed implementation overview.

A discussion of the model’s parameters follows.

## AC

The AC aspect of the model simulates the capacitive behavior of the inductor. A parallel capacitance, Cp, is inserted in parallel to model this effect. The parallel combination of the inductor and capacitor create a resonant frequency defined by:

$$fo = \frac{1}{2\pi\sqrt{Lo * Cp}}$$

This quantity is specified in datasheets and is entered in the **Inductor Self Resonant Frequency** field.

Magnetic loss, which dampens the resonant peak, is modeled with a parallel resistor, Rp. The relationship between Rp and the inductor quality factor Q, is:

$$Q = \frac{Rp}{2\pi fo Lo}$$

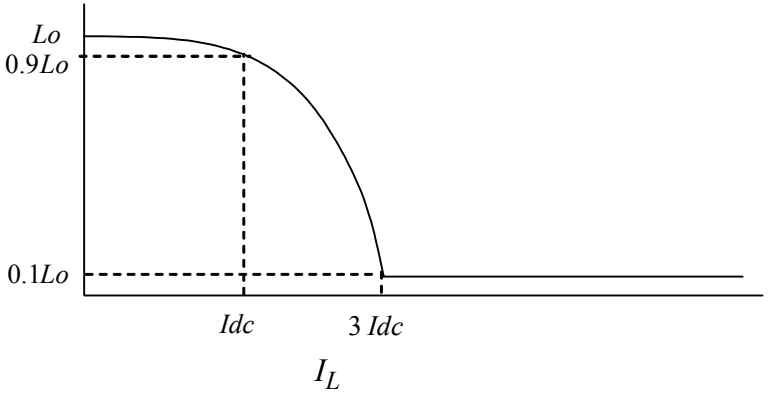
The inductor quality factor is also available in datasheets and is entered in the **Inductor Quality Factor** field.

## DC

The DC aspect of the model includes a series DC resistance, and a non-linear inductor whose inductance varies with current.

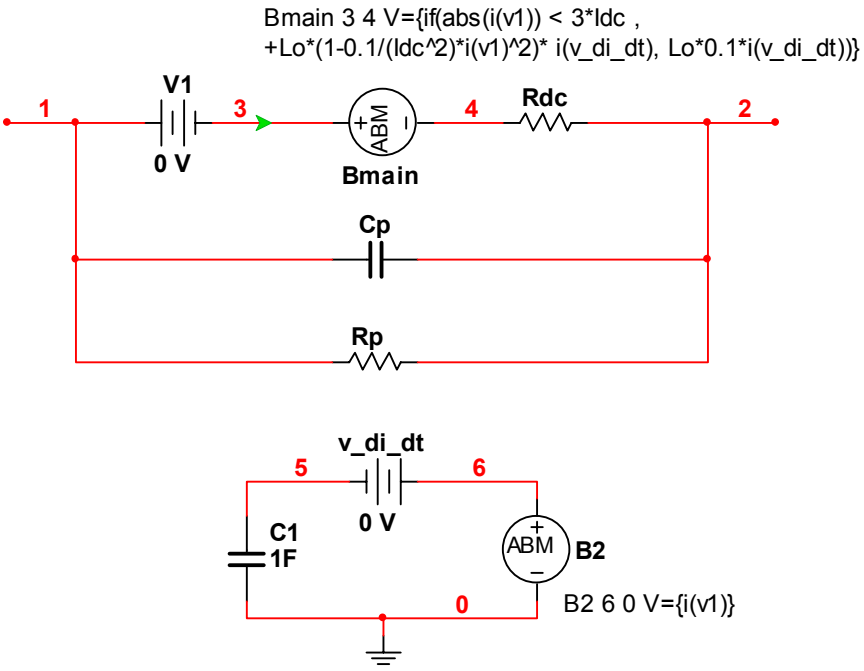
The DC resistance is the winding material resistance and is specified on the datasheet. It is entered in the **Inductor Series Resistance** field.

The non-linear inductance models the core's saturation using a second order polynomial. The polynomial coefficient is set such that when the inductor current reaches the rated current (Idc), the inductance has dropped to 90% of its nominal value, Lo. Both the nominal inductance and rated current can be found on the datasheet and are entered into the **Nominal Inductance** and **Inductor Rated Current** fields. The inductance value is clipped when it reaches 10% of the nominal value, to prevent the value from becoming negative.



## 2.9.1 Advanced Inductor Model Implementation

The schematic version of the advanced inductor SPICE model is shown below. Nodes 1 and 2 are the inductor's terminals.




Components Rdc, Cp, and Rp are parasitics that model the DC resistance and frequency response. The actual non-linear inductor is implemented using the Analog Behavioral Modeling (ABM) source, Bmain, and a secondary circuit. This is done by modeling the derivative operator, which is inherent to the inductor I/V relationship, with a unity-valued capacitor in a separate circuit.

The unity-valued capacitor is driven with a voltage value equal to the inductor current using ABM source B2, by referencing the current through the 0-volt source V1. In the expression of Bmain, the generated capacitor current (the derivative) is referenced through a 0 volt voltage source, v_di_dt.

Within the Bmain expression, the segment *Lo*(1-0.1/(Idc^2)*i(v1)^2)* v_di_dt* is exactly the inductor equation we desire:

$$V = Lo(1 - \frac{I_L^2}{10I_{dc}^2}) * \frac{dI_L}{dt}$$

The if-statement switches between the non-linear inductor model and the constant linear inductor model when the inductance falls to 10% of nominal value (or current has reached *3*Idc*).

References

[1] Martin O'Hara, "Modeling Non-Ideal Inductors in SPICE, Martin O'Hara," EETimes Asia, April 2002

# 2.10 Transformer

The transformer is one of the most common and useful applications of inductance. It can step up or step down an input primary voltage (V1) to a secondary voltage (V2). The relationship is given by V1/V2 = n, where n is the ratio of the primary turns to the secondary turns. The parameter n can be adjusted by editing the transformer's model.

To properly simulate the transformer, both sides must have a common reference point, which may be ground. The transformer can also be used in a center-tapped configuration. A center-tap is provided which may be used for this purpose. The voltage across the tap is half of the total secondary voltage.

This transformer is suitable for getting quick results. To simulate realistic devices that include a transformer, you should use the nonlinear transformer.

***Note*** Both sides of a transformer must be grounded.

## 2.10.1 Characteristic Equation

The characteristic equation of an ideal transformer is given by:

$$V_1 = nV_2$$

$$i_1 = \frac{1}{n} i_2$$

where:

$V_1$ = primary voltage

$V_2$ = secondary voltage

n = turns ratio

$i_1$ = primary current

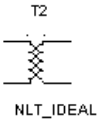
$i_2$ = secondary current

## 2.10.2 Ideal Transformer Model Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| n | Turns ratio | 2 | - |
| $L_e$ | Leakage inductance | 0.001 | H |
| $L_m$ | Magnetizing inductance | 5 | H |
| $R_p$ | Primary winding resistance | 0.0 | W |
| $R_s$ | Secondary winding resistance | 0.0 | W |

If n > 1, it is a step-down transformer; if n < 1, it is a step-up transformer.

# 2.11 Nonlinear Transformer




This component is based on a general model that can be customized for different applications.

It is implemented using a conceptual magnetic core and coreless coil building blocks, together with resistors and inductors. Using this transformer, you can model physical effects such as nonlinear magnetic saturation, primary and secondary winding losses, primary and secondary leakage inductances, and core geometric size.

See the “Magnetic Core” description for characteristic equations of the magnetic core.

## 2.11.1 Customizing

The nonlinear transformer can be customized for different applications. It is implemented by using a magnetic core and the coreless coil as the basic building blocks. The magnetic core takes in an input voltage and converts it to a Magnetomotive Force (mmf). The Magnetic Field Intensity (H) is calculated by dividing the mmf by the Length of the core:

H = mmf/L

H is then used to find the corresponding Flux Density (B). This is done by using the linear relationship described in the H-B array of coordinate pairs. This H-B array can be taken from the averaging H-B curve, which may be obtained from a technical manual that specifies the magnetic characteristics of different cores.

The slope of the B-H function is never allowed to change abruptly, but is smoothly varied whenever the Input Smoothing domain parameter is set to a number greater than zero.

The Flux Density (B) is multiplied by the cross-sectional area to obtain a Flux Value. The Flux Value is used by the coreless coil to obtain a value for the voltage reflected back across the terminals.

The core is modeled to be lossless. No core losses are considered. In the transformer model, the only losses taken into account are the ones modeled by the winding resistances.

To obtain the H-B points of the curve:

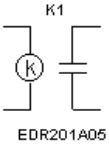
- Contact a manufacturing company. They many be able to provide the technical data required to model a core.
- Obtain experimental data.

## 2.11.2 Nonlinear Transformer Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| $N_1$ | Primary turns | 1 | - |
| $R_1$ | Primary resistance | 1e-06 | W |
| $L_1$ | Primary leakage inductance | 0.0 | H |
| $N_2$ | Secondary turns | 1 | - |
| $R_2$ | Secondary resistance | 1e-06 | W |
| $L_2$ | Secondary leakage inductance | 0.0 | H |

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| A | Cross-sectional area | 1.0 | $m^2$ |
| L | Core length | 1.0 | m |
| ISD | Input smoothing domain | 1.0% | - |
| N | Number of co-ordinates | | 2 |
| H1 | Magnetic field co-ordinate 1 | 0 | A*turns/m |
| H2 | Magnetic field co-ordinate2 | 1.0 | A*turns/m |
| H3-H15 | Magnetic field co-ordinates | 0 | A*turns/m |
| B1 | Flux density co-ordinate 1 | 0 | $Wb/m^2$ |
| B2 | Flux density co-ordinate 2 | 1.0 | $Wb/m^2$ |
| B3-B15 | Flux density co-ordinates | 0 | $Wb/m^2$ |

# 2.12 Relay




The magnetic relay can be used as a normally open or normally closed relay. It is activated when the current in the energizing circuit (attached to $P_1$, $P_2$) exceeds the value of the switch-on current (Ion). During operation, the contact switches from the normally closed terminals ($S_1$, $S_3$) to the normally open terminals ($S_1$, $S_2$). The relay will remain on as long as the current in the circuit is greater than the holding current ($I_{hd}$). The value of $I_{hd}$ must be less than that of $I_{on}$.

The magnetic relay is a coil with a specified inductance (Lc, in henries) that causes a contact to open or close when a specified current (Ion, in A) charges it.

The contact remains in the same position until the current falls below the holding value (Ihd, in A), at which point it returns to its original position.

## 2.12.1 Model

The energizing coil of the relay is modeled as an inductor, and the relay's switching contact is modeled as resistors $R_1$ and $R_2$.

## 2.12.2 Characteristic Equation

$R_1 = 0$

$R2 = \bullet$ *if* $i_p \leq i_{on}$

$R_1 = \bullet$

$R2 = 0$ *if* $i_{hd} < i_{on} \leq i_p$

where:

L = inductance of the relay energizing coil, in henrys

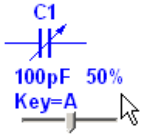
$R_{1,\ R2}$ = resistance of the relay's switching contact, in ohms

$i_{on}$ = turn-on current, in amperes

$i_{hd}$ = holding current, in amperes

$i_p$ = current through the energizing coil, in amperes

# 2.13 Variable Capacitor




The variable capacitor acts much like a regular capacitor, except that you can adjust its value using the keyboard or by hovering the cursor over the device and moving the slider bar that appears.

➢ To set up the variable capacitor:

1. Double-click on the variable capacitor and select the **Value** tab.
2. Enter the desired maximum capacitance for the device in the **Capacitance** field.
3. Enter the **Key** that will change the variable capacitor's value when pressed.

4. Enter the percentage by which you want the variable capacitor to change in the **Increment** field.
5. Optionally, enter **Component Type** and **Hyperlink** information.
6. Optionally, change the **Layout Settings** as described below:
   - **Edit Footprint** button — click to display the **Edit Footprint** dialog box where you can select a new **Footprint** and **Manufacturer**.

***Note*** For information on placing capacitors and variable capacitors, and information on how to edit footprints, refer to the *Multisim User Guide* or the Multisim helpfile.

- To increase the variable capacitor's value using the keyboard, press the identified key. The variable capacitor's setting will increase in steps the size of the value entered in the **Increment** field. For example, if the device is a 200 pF variable capacitor, and the **Increment** is set to 5%, its capacitance will increase by 10 pF steps until it reaches its maximum value of 200 pF.
- To decrease the value using the keyboard, press and hold SHIFT and press the identified key.

  For example, say the variable capacitor is set to 45%, the increment is 5% and the key is C. Press C , and the setting increases to 50%. Press C again, and it increases to 55%. Press SHIFT and C, and the setting decreases to 50%.
- To adjust the variable capacitor's value using the mouse:
  1. Hover the cursor over the device to display its slider bar.
  2. Drag the slider to the right to increase the value, or to the left to decrease the value.

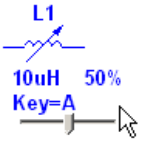
## Characteristic Equation and Model

This component's capacitance, *C*, is computed based on the initial settings according to the equation:

$$C = \frac{Setting}{100} * Capacitance$$

The variable capacitor is simulated as an open circuit with a current across the capacitor forced to zero by a large impedance value.

# 2.14 Variable Inductor




The variable inductor acts much like a regular inductor, except that you can adjust its value using the keyboard or by hovering the cursor over the device and moving the slider bar that appears.

➢ To set up the variable inductor:

1. Double-click on the variable inductor and select the **Value** tab.
2. Enter the desired maximum inductance for the device in the **Inductance** field.
3. Enter the **Key** that will change the variable inducotor's value when pressed.
4. Enter the percentage by which you want the variable inductor to change in the **Increment** field.
5. Enter the desired **Coil Resistance**.
6. Optionally, enter **Component Type** and **Hyperlink** information.
7. Optionally, change the **Layout Settings** as described below:
   - **Edit Footprint** button — click to display the **Edit Footprint** dialog box where you can select a new **Footprint** and **Manufacturer**.

***Note*** For information on placing inductors and variable inductors, and information on how to edit footprints, refer to the *Multisim User Guide* or the Multisim helpfile.

➢ To increase the variable inductor's value using the keyboard, press the identified key. The variable inductor's setting will increase in steps the size of the value entered in the **Increment** field. For example, if the device is a 200 uH variable capacitor, and the **Increment** is set to 5%, its inductance will increase by 10 uH steps until it reaches its maximum value of 200 uH.

➢ To decrease the value using the keyboard, press and hold SHIFT and press the identified key.

For example, say the variable inductor is set to 45%, the increment is 5% and the key is H. Press H , and the setting increases to 50%. Press H again, and it increases to 55%. Press SHIFT and H, and the setting decreases to 50%.

➢ To adjust the variable inductor's value using the mouse:

1. Hover the cursor over the device to display its slider bar.
2. Drag the slider to the right to increase the value, or to the left to decrease the value.

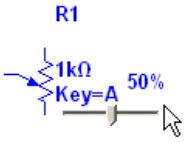
### Characteristic Equation and Model

This component's inductance, *L*, is computed based on the initial settings according to the equation:

$$L = \frac{Setting}{100} * Inductance$$

The variable inductor is simulated as an open circuit with a current across the inductor forced to zero by a large impedance value.

# 2.15 Potentiometer




The potentiometer acts much like a regular resistor, except that you can adjust its value using the keyboard or by hovering the cursor over the device and moving the slider bar that appears.

➢ To set up the potentiometer:

1. Double-click on the potentiometer and select the **Value** tab.
2. Enter the desired maximum resistance for the device in the **Resistance (R)** field.
3. Enter the **Key** that will change the potentiometer's value when pressed.
4. Enter the percentage by which you want the potentiometer to change in the **Increment** field.
5. Optionally, enter **Component Type** and **Hyperlink** information.
6. Optionally, change the **Layout Settings** as described below:
   - **Edit Footprint** button — click to display the **Edit Footprint** dialog box where you can select a new **Footprint** and **Manufacturer**.

***Note*** For information on placing resistors and potentiometers, and information on how to edit footprints, refer to the *Multisim User Guide* or the Multisim helpfile.

➢ To increase the potentiometer's value using the keyboard, press the identified key. The potentiometer's setting will increase in steps the size of the value entered in the **Increment** field. For example, if the device is a 200k linear potentiometer, and the **Increment** is set to 5%,

its resistance will increase by 10k steps until it reaches the potentiometer's maximum value of 200k ohms.

- To decrease the value using the keyboard, press and hold SHIFT and press the identified key.

  For example, say the potentiometer is set to 45%, the increment is 5% and the key is R. Press R, and the setting increases to 50%. Press R again, and it increases to 55%. Press SHIFT and R, and the setting decreases to 50%.

- To adjust the potentiometer's value using the mouse:

  1. Hover the cursor over the device to display its slider bar.
  2. Drag the slider to the right to increase the value, or to the left to decrease the value.

### Characteristic Equation and Model

The potentiometer is simulated using two resistors, $R_1$ and $R_2$, whose values are computed using the potentiometer's initial settings.

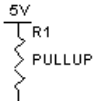
$$r = \frac{Setting}{100} * Resistance$$

where:

$R_1 = r$

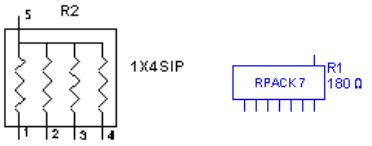
$R_2 = \text{Resistance} - r$

# 2.16 Pullup




This component is used to raise the voltage of a circuit to which it is connected. One end is connected to Vcc. The other end is connected to a point in a logic circuit that needs to be raised to a voltage level closer to Vcc.

# 2.17 Resistor Packs




Resistor packs are collections of resistors within a single package. The configuration of the resistors can be varied based on the intended usage of the package. Resistor packs are used to minimize the amount of space required on the PCB for the design. In some applications, noise can be a consideration for the use of resistor packs.

# 2.18 Voltage Controlled Resistor

The resistance of this device is controlled by the voltage that is applied across the "+" and "-" terminals. For every volt applied, the resistance increases by the amount set in the **Value** tab of the resistor's properties dialog. The default value is 1 kohm per volt. You can change this as desired in the **Resistance** field of the **Value** tab.

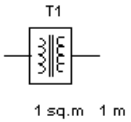
# 2.19 Voltage Controlled Capacitor

The capacitance of this device is controlled by the voltage that is applied across the "+" and "-" terminals. For every volt applied, the capacitance increases by the amount set in the **Value** tab of the capacitor's properties dialog. The default value is 1 farad per volt. You can change this as desired in the **Capacitance** field of the **Value** tab.

# 2.20 Voltage Controlled Inductor

The inductance of this device is controlled by the voltage that is applied across the "+" and "-" terminals. For every volt applied, the inductance increases by the amount set in the **Value** tab of the inductor's properties dialog. The default value is 1 henry per volt. You can change this as desired in the **Inductance** field of the **Value** tab.

# 2.21 Magnetic Core




This component is a conceptual model that you can use as a building block to create a wide variety of inductive and magnetic circuit models. Typically, you would use the magnetic core together with the coreless coil to build up systems that mock the behavior of linear and nonlinear magnetic components. It takes as input a voltage which it treats as a magnetomotive force (mmf) value.

## Characteristic Equation

Magnetic field intensity, H, is:

$H = mmf / l$

where:

$mmf$ = magnetomotive force, the input voltage

$l$ = core length

Flux density, B, is derived from a piecewise linear transfer function described to the model by the (magnetic field, flux density) pairs that you input in the Circuit/Component Properties dialog box. The final current, I, allowed to flow through the core is used to obtain a value for the voltage reflected back across the terminals. It is calculated as:

$I = BA$

where:

$A$ = cross-sectional area

### Magnetic Core Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *A* | Cross-sectional area | 1 | $m^2$ |
| *L* | Core length | 1 | m |
| *ISD* | Input smoothing domain% | 1 | - |
| *N* | Number of co-ordinates | 2 | - |
| *H1* | Magnetic field co-ordinate 1 | 0 | A·turns/m |
| *H2* | Magnetic field co-ordinate 2 | 1.0 | A·turns/m |
| *H3-H15* | Magnetic field co-ordinates | 0 | A·turns/m |
| *B1* | Flux density co-ordinate 1 | 0 | $Wb/m^2$ |
| *B2* | Flux density co-ordinate 2 | 1.0 | $Wb/m^2$ |
| *B3-B15* | Flux density co-ordinates | 0 | $Wb/m^2$ |

# 2.22 Coreless Coil




This component is a conceptual model that you can use as a building block to create a wide variety of inductive and magnetic circuit models. Typically, you would use the coreless coil together with the magnetic core to build up systems that mock the behavior of linear and nonlinear magnetic components. It takes as input a current and produces a voltage. The output voltage behaves like a magnetomotive force in a magnetic circuit, that is, when the coreless coil is connected to the magnetic core or some other resistive device, a current flows.

## 2.22.1 Characteristic Equation

$$V_{out} = N * i_{in}$$

where:

$V_{out}$ = output voltage value (magnetomotive force)

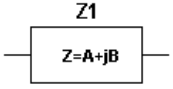
$i_{in}$ = input current

## 2.22.2 Coreless Coil Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *N* | Number of inductor turns | 1 | - |

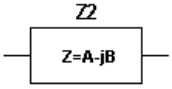
# 2.23 Z Loads

## 2.23.1 A+jB Block




The A+jB Block is a circuit block with resistance and inductance connected in series. "A" is resistance, "B" is inductive reactance ($X_L$) at a specified frequency and $j^2 = -1$. $X_L = 2\pi fL$, where f is the specified frequency and L is the inductance.

## 2.23.2 A-jB Block

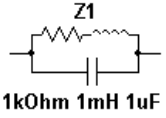



The A- jB Block is a circuit block with resistance and capacitance connected in series. "A" is resistance, "B" is capacitive reactance ($X_C$) at a specified frequency and $j^2 = -1$.

$$X_C = \frac{1}{2\pi fC}$$

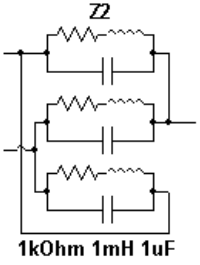
where f is the specified frequency and C is the capacitance.

## 2.23.3 Z Load 1



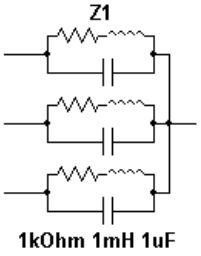

Z Load 1 is a circuit block with values of R, L and C as shown.

## 2.23.4 Z Load 1 Delta



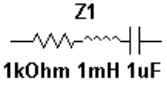

Z Load 1 Delta is a delta connection of three Z Load 1s as shown.

## 2.23.5 Z Load 1 Wye



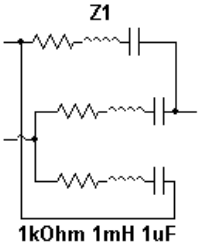

Z Load 1 Wye is a delta connection of three Z Load 1s as shown.

## 2.23.6 Z Load 2



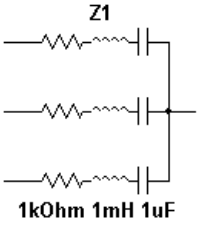

Z Load 2 is an RLC series connection block with R, L, and C values as shown.

## 2.23.7 Z Load 2 Delta



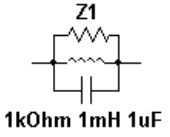

Z Load 2 Delta is a delta connection of three Z Load 2s as shown.

## 2.23.8 Z Load 2 Wye




Z Load 2 Wye is a wye connection of three Z Load 2s as shown.

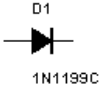
## 2.23.9 Z Load 3




Z Load 3 is a circuit block with an RLC parallel connection with R, L and C values as shown.

# Chapter 3
# Diodes

## 3.1 Diode




Diodes allow current to flow in only one direction and can therefore be used as simple solid-state switches in AC circuits, being either open (not conducting) or closed (conducting). Terminal A is called the anode and terminal K is called the cathode.

### 3.1.1 Diodes: Background Information

Diodes exhibit a number of useful characteristics, such as predictable capacitance (that can be voltage controlled) and a region of very stable voltage. They can, therefore, be used as switching devices, voltage-controlled capacitors (varactors) and voltage references (Zener diodes).

Because diodes will conduct current easily in only one direction, they are used extensively as power rectifiers, converting AC signals to pulsating DC signals, for both power applications and radio receivers.

Diodes behave as voltage-controlled switches, and have replaced mechanical switches and relays in many applications requiring remote signal switching.

Even indicator lamps are now replaced with diodes (LEDs) that emit light in a variety of colors when conducting.

A special form of diode, called a Zener diode, is useful for voltage regulation.

## 3.1.2 DC Model

The DC characteristic of a real diode in Multisim is divided into the forward and reverse characteristics.

DC forward characteristic:

$$I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right) + V_D * G_{\min} \quad \text{for } V_D \geq -5nV_T$$

DC reverse characteristic:

$$I_D = \begin{cases} I_S\left(e^{\frac{V_D}{nV_T}} - 1\right) + V_D * G_{\min} & \text{for } -5nV_T \leq V_D \leq 0 \\ -I_S + V_D * G_{\min} & \text{for } -BV < V_D < -5nV_T \\ -IBV & \text{for } V_D = -BV \\ -I_S\left(e^{-\left(\frac{BV+V_D}{V_T}\right)} - 1 + \frac{BV}{V_T}\right) & \text{for } V_D < -BV \end{cases}$$

where:

$I_D$ = current through the diode, in amperes

$V_D$ = voltage across the diode, in volts

$V_T$ = thermal voltage (= 0.0258 volts at room temperature (27°C))

BV = breakdown voltage

$I_S$ is equivalent to the reverse saturation current ($I_o$) of a diode. In a real diode, $I_S$ doubles for every 10-degree rise in temperature.

Other symbols used in these equations are defined in “Diode Parameters and Defaults”.

## 3.1.3 Time-Domain Model

This model defines the operation of the diode, taking into account its charge-storage effects or capacitance. There are two types of capacitances: diffusion or storage capacitance, and depletion or junction capacitance.

The charge-storage element, $C_{D,}$ takes into account both of these as follows:

$$C_D = \begin{cases} \tau_t \frac{dI_D}{dV_D} + C_{j0}\left(1 - \frac{V_D}{\varphi_0}\right)^{-m} & \text{for } V_D < FC * j_0 \\ \tau_t \frac{dI_D}{dV_D} + \frac{C_{j0}}{F_2}\left(F_3 + \frac{mV_D}{\varphi_0}\right) & \text{for } V_D \geq FC * j_0 \end{cases}$$

where:

$C_{j0}$ = zero-bias junction capacitance; typically 0.1 to 10 picofarads

$\varphi_0$ = junction potential; typically 0.5 to 0.7 volts

$\tau_t$ = transit time; typically 1 nanosecond

m = junction grading coefficient; typically 0.33 to 0.5

and where $F_2$ and $F_3$ are constants whose values are:

$$F_2 = (1 - FC)^{1+m}$$

$$F_3 = 1 - FC(1+m)$$

Notes

1. The voltage drop across the diode varies depending on the set value of:

   $I_S$ = saturation current; typically 10-14 amperes

   $r_S$ = ohmic resistance; typically 0.05 ohms.

2. The parameter $\tau_t$ is proportional to the reverse recovery time of the diode. That is, it affects the turn-off or switching speed of the diode. It is the time required for the minority carrier to cross the junction.

3. The barrier potential for a diode is approximately 0.7 to 0.8 volts. This is not to be confused with the model parameter $\varphi_0$ given above.

## 3.1.4 AC Small-Signal Model

The figure below shows the linearized, small-signal diode model, in which the diode is represented by a small-signal conductance, $g_D$. The small-signal capacitance is also evaluated at the DC operating point.

$$g_D = \frac{dI_D}{dV_D}\Big|_{OP} = \frac{I_S}{nV_T} e^{\frac{V_D}{nV_T}}$$

$$C_D = \frac{dQ_D}{dV_D}\Big|_{OP} = \begin{cases} \tau_t * g_D + C_{j0}\left(1 - \frac{V_D}{\varphi_0}\right)^{-m} & \text{for } V_D < FC * j_0 \\ \tau_t * g_D + \frac{C_{j0}}{F_2}\left(F_3 + \frac{mV_D}{\varphi_0}\right) & \text{for } V_D \geq FC * j_0 \end{cases}$$

where:

OP = operating point

$Q_D$ = the charge on $C_D$

## 3.1.5 Diode Parameters and Defaults

| Symbol | Parameter Name | Default | Typical Value | Unit |
|---|---|---|---|---|
| IS | Saturation current | 1e-14 | 1e-9 - 1e-18 cannot be 0 | A |
| RS | Ohmic resistance | 0 | 10 | W |
| CJO | Zero-bias junction capacitance | 0 | 0.01-10e-12 | F |
| VJ | Junction potential | 1 | 0.05-0.7 | V |
| TT | Transit time | 0 | 1.0e-10 | s |
| M | Grading coefficient | 0.5 | 0.33-0.5 | - |
| Symbol | Parameter Name | Default | Typical Value | Unit |

| Symbol | Parameter Name | Default | Typical Value | Unit |
|---|---|---|---|---|
| BV | Reverse bias breakdown voltage | 1e+30 | - | V |
| N | Emission coefficient | 1 | 1 | - |
| EG | Activation energy | 1.11 | 1.11 | eV |
| XTI | Temperature exponent for effect on *IS* | 3.0 | 3.0 | - |
| KF | Flicker noise coefficient | 0 | 0 | - |
| AF | Flicker noise exponent | 1 | 1 | - |
| FC | Coefficient for forward-bias depletion capacitance formula | 0.5 | 0.5 | - |
| IBV | Current at reverse breakdown voltage | 0.001 | 1.0e-03 | A |
| TNOM | Parameter measurement temperature | 27 | 27-50 | °C |

# 3.2 Pin Diode




The PIN diode consists of three semiconductor materials.

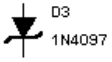
The center material is made up of intrinsic (pure) silicon. The *p*- and *n*-type materials are heavily doped and, as a result, have very low resistances.

When reverse biased, the PIN diode acts as a capacitor. The intrinsic material can be seen as the dielectric of a capacitor. The heavily doped *p*- and *n*-type materials can be viewed as the two conductors.

The intrinsic layer, which is a pure semiconductor with no impurities, makes the PIN diode respond better to infrared photons that penetrate deeper into the diode's regions.

The intrinsic layer creates a larger depletion region, which causes the diode to produce a more linear change in current in response to changes in light intensity.

# 3.3 Zener Diode




A zener diode is designed to operate in the reverse breakdown, or Zener, region, beyond the peak inverse voltage rating of normal diodes. This reverse breakdown voltage is called the Zener test voltage (Vzt), which can range between 2.4 V and 200 V.

In the forward region, it starts conducting around 0.7 V, just like an ordinary silicon diode. In the leakage region, between zero and breakdown, it has only a small reverse current. The breakdown has a sharp knee, followed by an almost vertical increase in current.

Zener diodes are used primarily for voltage regulation because they maintain constant output voltage despite changes in current.

## 3.3.1 DC Model

The DC characteristic of a real diode in Multisim is divided into the forward and reverse characteristics.

DC forward characteristic:

$$I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right) + V_D * G_{\min} \quad \text{for } V_D \geq -5nV_T$$

DC reverse characteristic:

$$I_D = \begin{cases} I_S\left(e^{\frac{V_D}{nV_T}} - 1\right) + V_D * G_{\min} & \text{for } -5\mathrm{nV_T} \leq \mathrm{V_D} \leq 0 \\ -I_S + V_D * G_{\min} & \text{for } -\mathrm{BV} < \mathrm{V_D} < -5\mathrm{nV_T} \\ -IBV & \text{for } \mathrm{V_D} = -\mathrm{BV} \\ -I_S\left(e^{-\left(\frac{BV+V_D}{V_T}\right)} - 1 + \frac{BV}{V_T}\right) & \text{for } \mathrm{V_D} < -\mathrm{BV} \end{cases}$$

where:

$I_D$ = current through the diode in amperes

$V_D$ = voltage across the diode in volts

$V_T$ = thermal voltage (= 0.0258 volts at room temperature (27°C))

BV = breakdown voltage

$I_S$ is equivalent to the reverse saturation current ($I_o$) of a diode. In a real diode, $I_S$ doubles for every 10-degree rise in temperature.

Other symbols used in these equations are defined in the table below.

## 3.3.2 Zener Diode Parameters and Defaults

| Symbol | Parameter name | Default | Unit |
|---|---|---|---|
| Is | Saturation current | 1e-14 | A |
| Rs | Ohmic resistance | 0 | W |
| CJO | Zero-bias junction capacitance | 0 | F |
| VJ | Junction potential | 1 | V |
| TT | Transit time | 0 | S |
| M | Grading coefficient | 0.5 | - |
| VZT | Zener test voltage | 1e+30 | V |
| IZT | Zener test current | 0.001 | A |
| N | Emission coefficient | 1 | - |
| EG | Activation energy | 1.11 | eV |
| XTI | Temperature exponent for effect on Is | 3.0 | - |
| Symbol | Parameter name | Default | Unit |
| KF | Flicker noise coefficient | 0 | - |
| AF | Flicker noise exponent | 1 | - |

| Symbol | Parameter name | Default | Unit |
|---|---|---|---|
| FC | Coefficient for forward-bias depletion capacitance formula | 0.5 | - |
| TNOM | Parameter measurement temperature | 27 | °C |

# 3.4 LED (Light-Emitting Diode)



This diode emits visible light when forward current through it, $I_{d,}$ exceeds the turn-on current, $I_{on}$.

LEDs are used in the field of optoelectronics. Infrared devices are used together with spectrally matched phototransistors in optoisolation couplers, hand-held remote controllers, and in fiber-optic sensing techniques. Visible spectrum applications include status indicators and dynamic power level bar graphs on a stereo system or tape deck.

## 3.4.1 Background Information

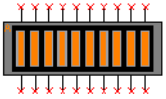
LEDs are constructed of gallium arsenide or gallium arsenide phosphide. While efficiency can be obtained when conducting as little as 2 milliamperes of current, the usual design goal is in the vicinity of 10 mA. During conduction, there is a voltage drop across the diode of about 2 volts.

Most early information display devices required power supplies in excess of 100 volts. The LED ushered in an era of information display components with sizes and operating voltages compatible with solid-state electronics. Until the low-power liquid-crystal display was developed, LED displays were common, despite high current demands, in battery-powered instruments, calculators and watches. They are still commonly used as on-board annunciators, displays and solid-state indicator lamps.

### 3.4.2 LED Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| IS | Saturation current | 1e-14 | A |
| RS | Ohmic resistance | 0 | W |
| CJO | Zero-bias junction capacitance | 0 | F |
| VJ | Junction potential | 1 | V |
| TT | Transit time | 0 | s |
| M | Grading coefficient | 0.5 | - |

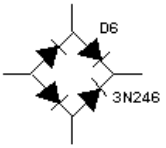
## 3.5 Bar LED



The bar LED comes in assorted colors and 4-, 8-, and 10-segment sizes.

To adjust the **On Current (Ion)**, double-click on the component and select the **Value** tab.

# 3.6 Full-Wave Bridge Rectifier




The full-wave bridge rectifier uses four diodes to perform full-wave rectification of an input AC voltage. Two diodes conduct during each half cycle, giving a full-wave rectified output voltage. The top and bottom terminals can be used as the input terminals for the AC voltage. The left and right terminals can be used as the output DC terminals.

## 3.6.1 Characteristic Equation

The average output DC voltage at no load condition is approximately given by:

$V_{DC} = 0.636 * (Vp - 1.4)$

where:

$V_p$ = the peak value of the input AC voltage

## 3.6.2 Model

A full-wave bridge rectifier consists of four diodes as shown in its icon.

Terminals 1 and 2 are the input terminals, so the input AC source is connected across 1 and 2. Terminals 3 and 4 are the output terminals, so the load is connected across 3 and 4.

When the input cycle is positive, diodes $D_1$ and $D_2$ are forward-biased and $D_3$ and $D_4$ are reverse-biased. $D_1$ and $D_2$ thus conduct current in the direction shown. The voltage developed is identical to the positive half of the input sine wave minus the diode drops.

When the input cycle is negative, diodes $D_3$ and $D_4$ become forward-biased and conduct current in the direction shown. Hence, the current flows in the same direction for both the positive and the negative halves of the input wave. A full-wave rectified voltage appears across the load.

## 3.6.3 Full-Wave Bridge Rectifier Parameters and Defaults

| Symbol | Parameter Name | Default | Typical Value | Unit |
|---|---|---|---|---|
| IS | Saturation current | 1e-14 | 1e-9 - 1e-18 cannot be 0 | A |
| RS | Ohmic resistance | 0 | 10 | W |
| CJO | Zero-bias junction capacitance | 0 | 0.01-10e-12 | F |
| VJ | Junction potential | 1 | 0.05-0.7 | V |
| TT | Transit time | 0 | 1.0e-10 | s |
| M | Grading coefficient | 0.5 | 0.33-0.5 | - |
| BV | Reverse bias breakdown voltage | 1e+30 | - | V |
| N | Emission coefficient | 1 | 1 | - |
| EG | Activation energy | 1.11 | 1.11 | eV |
| XTI | Temperature exponent for effect on *IS* | 3.0 | 3.0 | - |
| KF | Flicker noise coefficient | 0 | 0 | - |
| AF | Flicker noise exponent | 1 | 1 | - |
| FC | Coefficient for forward-bias depletion capacitance formula | 0.5 | 0.5 | - |
| IBV | Current at reverse breakdown voltage | 0.001 | 1.0e-03 | A |
| TNOM | Parameter measurement temperature | 27 | 27-50 | °C |

# 3.7 Schottky Diode




The Schottky diode is a two-terminal device with a junction that uses metal in place of the *p*-type material. The formation of a junction with a semiconductor and metal results in very little junction capacitance.

The Schottky diode will have a $V_F$ of approximately 0.3 V and a $V_{BR}$ of less than − 50 V. These are lower than the typical *pn*-junction ratings of $V_F = 0.7$ V and $V_{BR} = -1$ 50 V.

With very little junction capacitance, the Schottky diode can be operated at much higher frequencies than the typical *pn*-junction diode and has a much faster switching time.

The Schottky diode is a relatively high-current device that is capable of switching rapidly while providing forward currents of approximately 50 A. It can operate at frequencies of 20 GHz and higher in sinosoidal and low-current switching circuits.

# 3.8 Silicon-Controlled Rectifier




A silicon-controlled rectifier (SCR) is a unidirectional current control device like a Shockley diode. However, the SCR has a third terminal capable of supporting a digital gate connection, which adds another means of controlling the current flow. The SCR switches on when the forward bias voltage exceeds the forward-breakover voltage or when a current pulse is applied to the gate terminal.

The SCR is triggered into conduction by applying a gate-cathode voltage (*VGK*), which causes a specific level of gate current (*IG*). The gate current triggers the SCR into conduction. The device is returned to its nonconducting state by either anode current interruption or forced commutation. When the SCR is turned off, it stays in a non-conducting state until it receives another trigger.

## 3.8.1 Model

The SCR is simulated using a mixed electrical and behavioral model.

The status of the SCR is handled with a logical variable, much like the Shockley diode and diac simulations. The resistance, $R_{s,}$ acts as a current block when the SCR is switched off. $R_S$ has two separate values, depending on the status of the SCR. When the SCR is on, the resistance $R_S$ is low; when the SCR is off, the resistance $R_S$ is high. The high resistance value acts as a current block.

The SCR is switched on and $R_s$ set low (*1e-06*) if:

$$Vd \geq Vdrm$$

or

$$Ig \geq Igt \; at \; Vg \geq Vgt \text{ and}$$

$$Vd \geq 0$$

or

$$\frac{dV_d}{dt} \geq \frac{dV}{dt} \quad \text{of the SCR}$$

The SCR is switched off and $R_s$ set high if:

$$Id < \mathrm{I}h$$

In this case, the switching occurs after turn-off time $T_{q,}$ which is implemented by the behavioral controller.

$I_d$ = current through the SCR, in amperes

$r_s$ = blocking resistance, in ohms

Symbols used in these equations are defined in “SCR Parameters and Defaults”.

## 3.8.2 Time-Domain Model

For the time-domain model, the charge-storage effects of the SCR junction capacitance are considered in the simulation.

The turn-off time, $T_{q,}$ is implemented by introducing a behavioral delay in the opening of the controlled switch.

## 3.8.3 AC Small-Signal Model

In the AC model, the diode is represented by its linearized small-signal model. The diode small-signal conductance $g_d$ and the small-signal capacitance Cd are evaluated at the DC operating point.

## 3.8.4 SCR Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| Irdm | Peak off-state current | 1e-06 | A |
| Vdrm | Forward breakover voltage | 200 | V |
| Vtm | Peak on-state voltage | 1.5 | V |
| Itm | Forward current at which Vtm is measured | 1 | A |
| Tq | Turn-off time | 1.5e-05 | s |
| dv/dt | Critical rate of off-state voltage rise | 50 | $V/\mu s$ |
| Ih | Holding current | 0.02 | A |
| Vgt | Gate trigger voltage | 1 | V |
| Igt | Gate trigger current | 0.001 | A |
| Vd | Voltage at which Igt is measured | 10 | V |

# 3.9 DIAC




A diac is a two-terminal parallel-inverse combination of semiconductor layers that allows triggering in either direction. It functions like two parallel Shockley diodes aligned back-to-back. The diac restricts current flow in both directions until the voltage across the diac exceeds the switching voltage. Then the diac conducts current in the direction of the voltage.

## 3.9.1 DC Model

The diac is switched on and the resistance, $R_{s,}$ is set low if, in either the positive or negative direction.

$$V_d \geq V_s$$

The diac is switched off (current-blocking mode) and $R_s$ is set high if, in either direction:

$$\frac{V_s}{I_{rev}}$$

$$Id < Ih$$

where:

$V_d$ = voltage across the diac, in volts

$I_d$ = current through the diac, in amperes

$R_s$ = blocking resistance

$I_{rev}$ = = peak off-state reverse current

Other symbols used in these equations are defined in “Diac Parameters and Defaults”.

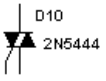
## 3.9.2 Time-Domain and AC Small-Signal Models

Each of the Shockley diodes is simulated with the mixed electrical/behavioral model described in the DC model above.

## 3.9.3 DIAC Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| IS | Saturation current | 1e-06 | A |
| Vs | Switching voltage | 100 | V |
| Vtm | Peak on-state voltage | 1.5 | V |
| Itm | Forward current at which Vtm is measured | 1 | A |
| Tq | Turn-off time | 1e-06 | s |
| Ih | Holding current | 0.02 | A |
| CJO | Zero-bias junction capacitance | 1e-12 | F |

# 3.10 TRIAC




A triac is a three-terminal five-layer switch capable of conducting current in both directions. The triac model consists of two SCRs, each of which is modeled as described earlier in this chapter. The triac remains off, restricting current in both directions until the voltage across the triac exceeds the breakover voltage, or until a positive pulse of current is applied to the gate terminal.

## 3.10.1 Model

The simulation is a combined electrical/behavioral model. The status of the triac, either on or off, is treated as a logical variable. The resistance, $R_{s,}$ is a function of the triac status.

When the triac is off, the resistance $R_s$ is set high to act as a current block. When the triac is on, $R_S$ is low (*1e-06*).

$$\left(\frac{V_{drm}}{I_{drm}}\right)$$

The triac is switched on in either direction if:

$Vd \geq Vdrm$

Rs = 1e - 06

or

$Vd \geq 0$ and

Ig ≥ Igt at Vg ≥ Vgt

or $\frac{dV_d}{dt} \geq \frac{dV}{dt}$ of the triac

The triac is switched off and the resistance $R_s$ is set high (current-blocking mode) if:

Id < Ih

In this case the switching occurs after turn-off time $T_q$, which is implemented by the behavioral controller.

Vs = maximum forward breakover voltage, or switching voltage, in volts

$I_d$ = current through the diac, in amperes

$R_s$ = blocking resistance, in ohms

$I_{rev}$ = peak off-state reverse current

$v_{br}$ = maximum forward breakover voltage, in volts

$i_d$ = current through the triac, in amperes

Vd = voltage across the diac, in volts

vd = voltage across the triac, in volts

$t_d$ = turn-on time, in seconds

Other symbols used in these equations are defined in “Triac Parameters and Defaults”.

# 3.11 Varactor Diode




The varactor is a type of *pn*-junction diode with relatively high junction capacitance when reverse biased. The capacitance of the junction is controlled by the amount of reverse voltage applied to the device, which makes the device function as a voltage-controlled capacitor.

The capacitance of a reverse-biased varactor junction is found in the following way:

$$C_T = (\varepsilon)\frac{A}{W_d}$$

where:

$C_T$ = the total junction capacitance

$\varepsilon$ = permittivity of the semiconductor material

$A$ = the cross-sectional area of the junction

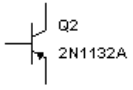
$W_d$ = the width of the depletion layer

The value of $C_T$ is inversely proportional to the width of the depletion layer. The depletion layer acts as an insulator (called the dielectric) between the *p*-type and *n*-type materials.

Varactor diodes are used in place of variable capacitors in many applications.

# Chapter 4
# Transistors

## 4.1 BJT (NPN & PNP)




A bipolar junction transistor, or BJT, is a current-based valve used for controlling electronic current. BJTs are operated in three different modes, depending on which element is common to input and output: common base, common emitter or common collector. The three modes have different input and output impedances and different current gains, offering individual advantages to a designer.

A transistor can be operated in its nonlinear region as a current/voltage amplifier or as an electronic switch in cutoff and saturation modes. In its linear region, it must be biased appropriately (i.e., subjected to external voltages to produce a desired collector current) to establish a proper DC operating point. The transistors' parameters are based on the Gummel-Poon transistor model.

BJTs are commonly used in amplification and switching applications. They come in two versions: NPN and PNP. The letters refer to the polarities, positive or negative, of the materials that make up the transistor sandwich. For both NPNs and PNPs, the terminal with the arrowhead represents the emitter.

An NPN transistor has two n-regions (collector and emitter) separated by a p-region (base). The terminal with the arrowhead is the emitter. The ideal NPN in the parts bin has generic values suitable for most circuits. You can specify a real-world transistor by double-clicking the icon and choosing another model.

A PNP transistor has two p-regions (collector and emitter) separated by an n-region (base). The terminal with the arrowhead represents the emitter. The ideal PNP model has generic values suitable for most circuits. You can specify a real-world transistor by double-clicking the icon and choosing another model.

## 4.1.1 Characteristic Equations

$$I_E = I_C + I_B$$

$$\beta_{DC} = \frac{I_C}{I_B} = h_{FE}$$

$$\beta_{AC} = \frac{\Delta I_C}{\Delta I_B} = \left| \; OP(V_{CE}) = h_{fe} \right.$$

where:

$\beta_{DC} = h_{FE}$ = DC current gain

$\beta_{AC} = h_{fe}$ = small-signal current gain

$I_C$ = collector current

$I_B$ = base current

$\Delta I_E$ = emitter current

The model for the PNP transistor is the same as the NPN model, except the polarities of the terminal currents and voltages are reversed.

The DC characteristic of a BJT in Multisim is modeled by a simplified Gummel-Poon model. The base-collector and base-emitter junctions are described by their ideal diode equations. The diode capacitors are treated as open circuits.

The beta variation with current is modeled by two extra non-ideal diodes. The diode capacitors are treated as open circuits. The various equations are:

$$I_{BE2} = I_{SE}\left[ \exp\left( \frac{V_{BE}}{n_e V_T} \right) - 1 \right]$$

$$I_{BC2} = I_S\left[ \exp\left( \frac{V_{BC}}{n_c V_T} \right) - 1 \right]$$

$$K_{q1} = \frac{1}{1 - \frac{V_{BC}}{VA}}$$

$$K_{q2} = \frac{I_S}{IKF}\left[ \exp\left( \frac{V_{BE}}{V_T} \right) - 1 \right]$$

$$K_{qb} = \frac{K_{q1}}{2}\left( 1 + \sqrt{1 + 4K_{q2}} \right)$$

$$I_{CE} = \frac{I_S}{K_{qb}}\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right]$$

$$I_{CC} = \frac{I_S}{K_{qb}}\left[\exp\left(\frac{V_{BC}}{V_T}\right) - 1\right]$$

$$I_{CT} = I_{CE} - I_{CC}$$

$$I_{BE1} = I_S\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right]$$

$$I_{BC1} = I_S\left[\exp\left(\frac{V_{BC}}{V_T}\right) - 1\right]$$

where:

$V_T$ = thermal voltage = 0.0258

$V_A$ = forward early voltage

The model parameter $\beta_f$ is equivalent to $\beta_{DC}$ in the DC case and $\beta_{AC}$ in the AC case.

Other symbols used in these equations are defined in "BJT Model Parameters and Defaults."

## 4.1.2 Time-Domain Model

The BJT time-domain model takes into account the parasitic emitter, base and collector resistances, and also the junction, diffusion, and substrate capacitances. The capacitors in the

model are represented by their energy storage model derived using the appropriate numerical integration rule.

$$C_{BE} = \begin{cases} \tau_F \frac{dI_{CC}}{dV_{BE}} + C_{jE0}\left(1 - \frac{V_{BE}}{\varphi_E}\right)^{-m_E} & \text{for } V_{BE} < FC*\varphi_E \\ \tau_F \frac{dI_{CC}}{dV_{BE}} + \frac{C_{jE0}}{F_2}\left(F_3 + \frac{m_E V_{BE}}{\varphi_E}\right) & \text{for } V_{BE} \geq FC*\varphi_E \end{cases}$$

$$C_{BC} = \begin{cases} \tau_R \frac{dI_{EC}}{dV_{BC}} + C_{jC0}\left(1 - \frac{V_{BC}}{\varphi_C}\right)^{-m_C} & \text{for } V_{BC} < FC*\varphi_C \\ \tau_R \frac{dI_{EC}}{dV_{BC}} + C_{jC0}\left(F_3 + \frac{m_C V_{BC}}{\varphi_C}\right) & \text{for } V_{BC} \geq FC*\varphi_C \end{cases}$$

$$C_{sub} = \begin{cases} C_{js0}\left(1 - \frac{V_{CS}}{\varphi_S}\right)^{-m_s} & \text{for } V_{Cs} < 0 \\ C_{js0}\left(1 + \frac{m_s V_{CS}}{\varphi_s}\right) & \text{for } V_{Cs} > 0 \end{cases}$$

$$C_{JX} = \begin{cases} C_{jC0}\left(1\text{-}X_{CJC}\right)\left(1 - \frac{V_{BX}}{\varphi_C}\right)^{-m_C} & \text{for } V_{BX} < FC*\varphi_C \\ \frac{C_{jC0}\left(1\text{-}X_{CJC}\right)}{F_2} * \left(F_3 + \frac{m_C V_{BX}}{\varphi_C}\right) & \text{for } V_{BX} \geq FC*\varphi_C \end{cases}$$

where, for the base-emitter junction, $C_{BE}$,

$$F_2 = (1 - FC)^{1+m_E}$$

$$F_3 = 1 - FC(1 + m_E)$$

and for the base-collector junction, $C_{BC}$ and $C_{JX}$,

$$F_2 = \left(1 - FC\right)^{1+m_C}$$

$$F_3 = 1 - FC\left(1 + m_C\right)$$

The symbols used in these equations are defined in "BJT Model Parameters and Defaults."

## 4.1.3 AC Small-Signal Model

The small-signal model of a BJT is automatically computed during linearization of the DC and large-signal time-domain models. The circuit shown is the Gummel-Poon small-signal model of an NPN transistor.

$$C_\pi = C_{BE}\,|_{\,OP} \qquad g_\pi = \frac{I_B}{V_T}|_{\,OP}$$

$$C_\mu = C_{BC}\,|_{\,OP} \qquad g_m = \frac{I_C}{V_T}|_{\,OP}$$

$$C_s = C_{sub}\,|_{\,OP} \qquad g_0 = \frac{I_c}{V_A}|_{\,OP}$$

$$C_{JX} = C_{JX}\,|_{\,OP} \qquad \beta_{ac}\frac{g_m}{g_\pi}$$

$$i_c = g_\pi v_{be} + g_\mu v_{ce}$$

where:

$g_p$ = input conductance

$g_\mu$ = reverse feedback conductance

$g_m$ = transductance

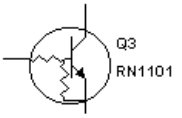
$g_o$ = output conductance.

# 4.1.4 BJT Model Parameters and Defaults

| Symbol | Parameter Name | Default | Example | Unit |
|---|---|---|---|---|
| IS | Saturation current | 1e-16 | 1e-15 | A |
| $\beta F$ | Forward current gain coefficient | 100 | 100 | - |
| $\beta R$ | Reverse current gain coefficient | 1 | 1 | - |
| rb | Base ohmic resistance | 0 | 100 | W |
| re | Emitter ohmic resistance | 0 | 10 | W |
| rc | Collector ohmic resistance | 0 | 1 | W |
| Cs | Substrate capacitance | 0 | 1 | F |
| Ce, Cc | Zero-bias junction capacitances | 0 | 2e-09 | F |
| $\phi e, \phi c$ | Junction potentials | 0.75 | 0.75 | V |
| $\tau F$ | Forward transit time | 0 | 1e-13 | s |
| $\tau R$ | Reverse transit time | 0 | 10e-09 | s |
| me, mc | Junction grading coefficients | 0.33 | 0.5 | - |
| VA | Early voltage | 1e+30 | 200 | V |
| Ise | Base emitter leakage saturation current | 0 | 1e-13 | A |
| Ikf | Forward beta high-current knee-point | 1e+30 | 0.01 | A |
| Ne | Base-emitter leakage emission coefficient | 1.5 | 2 | - |
| NF | Forward current emission coefficient | 1 | 1 | - |
| NR | Reverse current emission coefficient | 1 | 1 | - |
| VAR | Reverse early voltage | 1e+30 | 200 | V |
| IKR | Reverse beta roll-off corner current | 1e+30 | 0.01 | A |
| ISC | B-C leakage saturation current | 0 | 0.01 | A |
| NC | B-C leakage emission coefficient | 2 | 1.5 | - |

| Symbol | Parameter Name | Default | Example | Unit |
|---|---|---|---|---|
| IRB | Current for base resistance equal to (rb+RBM)/2 | 1e+30 | 0.1 | A |
| RBM | Minimum base resistance at high currents | 0 | 10 | W |
| XTF | Coefficient for bias dependence of tF | 0 | 0 | - |
| VTF | Voltage describing VBC dependence of tF | 1e+30 | - | V |
| ITF | High current dependence of tF | 0 | - | A |
| PTF | Excess phase at frequency equal to 1/(tF*2PI) Hz | 0 | - | Deg |
| XCJC | Fraction of B-C depletion capacitance connected to internal base node | 1 | - | - |
| VJS | Substrate junction build-in potential | .75 | - | V |
| MJS | Substrate junction exponential factor | 0 | 0.5 | - |
| XTB | Forward and reverse beta temperature exponent | 0 | - | - |
| EG | Energy gap for temperature effect on IS | 1.11 | - | eV |
| XTI | Temperature exponent for effect on IS | 3 | - | - |
| KF | Flicker noise coefficient | 0 | - | - |
| AF | Flicker noise exponent | 1 | - | - |
| FC | Coefficient for forward-bias depletion capacitance formula | .5 | - | - |
| TNOM | Parameter measurement temperature | 27 | 50 | °C |

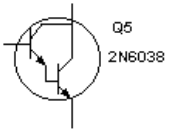
# 4.2 Resistor Biased BJT (NPN & PNP)




Resistor biased BJTs are discrete transistors which have had additional resistors added to them within a standard transistor package. This is done to reduce the space required on the PCB for the design. The general application is for transistor switches for displays such as LED and Hex displays.

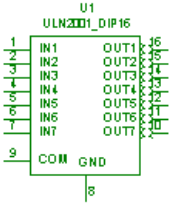
They come in two varieties: with a NPN transistor or a PNP transistor.

# 4.3 Darlington Transistor (NPN & PNP)




The Darlington connection is a pair of two bipolar junction transistors for operation as a composite transistor. The composite transistor acts as a single unit with a current gain that is the product of the current gains of each bipolar junction transistor.

A Darlington array consists of seven Darlington pairs. Each pair has an input and an output. There is also one Common and one GND pin on the IC.



## 4.3.1 DC Bias Model

If a Darlington transistor with a very high current gain, $\beta_D$, is used, the base current may be calculated from

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$$

This equation is the same for a regular transistor, however, the value of $\beta_D$ is much greater, and the value of $V_{BE}$ is larger.

The emitter current is then

$$I_E = (\beta_D + 1) I_B \approx \beta_D I_B$$

DC voltages are:

$$V_E = I_E R_E$$

$$V_B = V_E + V_{BE}$$

## 4.3.2 AC Model

The AC input signal is applied to the base of the Darlington transistor through capacitor $C_1$, with the ac output, $V_o$, obtained from the emitter through capacitor $C_2$. The Darlington transistor is replaced by an ac equivalent circuit made up of an input resistance, $r_i$, and an output current source, $\beta_D I_b$.

### 4.3.2.1 AC Input Impedance

The AC input impedance looking into the transistor base is then

$$\frac{V_i}{I_b} = r_i + \beta_D R_E$$

The AC input impedance looking into the circuit is

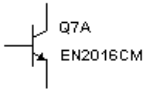
$$Z_i = R_B \parallel (r_i + \beta_D R_E)$$

#### 4.3.2.2 AC Current Gain

The AC circuit gain is as follows:

$$A_i = \beta_D \frac{R_B}{R_B + \beta_D R_E} = \frac{\beta_D R_B}{R_B + \beta_D R_E}$$

## 4.4 BJT Array




BJT arrays are collections of discrete transistors on a single die. They can come in many variations based on their intended application. The reasons for using an array is that the devices are more closely matched than a random group of discrete devices (eliminating the need to sort them), the noise characteristics are better, and the space required on a PCB is smaller.

There are three types of BJT arrays:

- PNP transistor array
- NPN/PNP transistor array
- NPN transistor array.

### 4.4.1 General-purpose PNP Transistor Array

This general-purpose silicon PNP transistor array incorporates two transistors, a Darlington circuit, and a current-mirror pair with a shared diode.

The two transistors can be used in circuit applications. The total array can be used in applications in systems with low-power and low-frequency requirements.

### 4.4.2 NPN/PNP Transistor Array

This general-purpose high-voltage silicon transistor array consists of five independent transistors (two PNP and three NPN types) on a common substrate, which has a separate connection. Separate connection for each transistor permits greater flexibility in circuit design.

This array is useful in applications including differential amplifiers, DC amplifiers, level shiftors, timers, thyristor firing circuits and operational amplifiers.

### 4.4.3 General-purpose High-current NPN Transistor Array

This array consists of five high-current NPN transistors on a common monolithic substrate. Two of these transistors are matched at low currents for applications in which offset parameters are particularly important. Independent connections for each transistor and a separate terminal for the substrate allow for maximum flexibility in circuit design.

This array is useful in applications such as signal processing and switching systems operating from DC to VHF. Other applications include lamp and relay driver, differential amplifier, thyristor firing and temperature-compensated amplifier.

## 4.5 P-Channel MOSFET

This device is a P-channel MOSFET. See also “MOSFET” on page 4-11.

## 4.6 N-Channel MOSFET

This device is an N-channel MOSFET. See also “MOSFET” on page 4-11.

## 4.7 MOSFET

A MOSFET is a Metal-Oxide-Semiconductor FET. This transistor is a type of FET that uses an induced electrical field to control current through the device. Either negative or positive gate voltages can be applied to control the current.

The substrate is usually connected to the most negatively biased part of the MOSFET, usually the source lead. In the three-terminal MOSFETs, the substrate is internally connected to the source. N-channel MOSFETs have an inward-pointing substrate arrow, and p-channel MOSFETs have an outward-pointing arrow. N-channel and p-channel MOSFETs are identical, except that their voltage polarities are opposite.

The 4-Terminal Enhanced N-MOSFET is an n-channel enhancement MOSFET. Because the substrate lead is not connected to the source lead, it has four terminals.

The 4-Terminal Enhanced P-MOSFET is a p-channel enhancement MOSFET. Because the substrate and source leads are not connected, it has four terminals.

## 4.7.1 Depletion MOSFETs

Like a JFET, a depletion MOSFET consists of a length of p-type (for a p-channel MOSFET) or n-type (for an n-channel MOSFET) semiconductor material, called the channel, formed on a substrate of the opposite type. The gate is insulated from the channel by a thin silicon dioxide ($SiO_{2)}$ layer. Depletion MOSFETs are used in automatic-gain control (AGC) circuits.

## 4.7.2 Enhancement MOSFETs

An enhancement MOSFET has no physical channel between the drain and the source, unlike the depletion MOSFET. Instead, the substrate extends all the way to the silicon dioxide ($SiO_{2)}$ layer. An enhancement MOSFET works only with positive gate-source voltages. Enhancement MOSFETs are extensively used in digital circuits and large-scale integration (LSI) applications.

Multisim provides four MOSFET device models, which differ in the formulation of the current-voltage characteristic. The parameter LEVEL in the model dialog specifies the model to be used. LEVEL 1 is a modified Shichman-Hodges model. LEVEL 2 defines the geometry-based analytical model. LEVEL 3 defines the semi-empirical short-channel model. LEVEL 4 defines the BS1M1 model. LEVEL 5 defines a new BS1M2 model.

## 4.7.3 DC Model

Due to the complexity of the MOSFET models used, only very basic formulas are provided in the following description.

The DC characteristics are modeled by a nonlinear current source, $I_{D.}$

Forward characteristics ($V_{DS \geq 0)}$:

$$V_{TE} = V_{TO} + \gamma\left(\sqrt{\varphi - V_{BS}}\right) - \sqrt{\varphi} \qquad \text{for } \gamma > 0, \varphi > 0$$

$$I_D = \begin{cases} 0 & \text{for } (V_{GS} - VE) \le 0 \\ \beta(V_{GS} - V_{TE})^2(1 + \lambda V_{DS}) & \text{for } 0 < (V_{GS} - V_{TE}) \le V_{DS} \\ \beta(V_{DS}[2(V_{GS} - V_{TE}) - V_{DS}](1 + \lambda V_{DS}) & \text{for } 0 < V_{DS} \le (V_{GS} - V_{TE}) \end{cases}$$

Reverse characteristics ($V_{DS} < 0$):

$$V_{TE} = V_{TO} = \gamma\left(\sqrt{\varphi - V_{BD}}\right) - \sqrt{\varphi}$$

$$I_D = \begin{cases} 0 & \text{for } (V_{GD} - V_{TE}) \le 0 \\ -\beta(V_{GS} - V_{TE})^2(1 - \lambda V_{DS}) & \text{for } 0 < (V_{GD} - V_{TE}) \le -V_{DS} \\ \beta(V_{DS}[2(V_{GD} - V_{TE}) + V_{DS}](1 - \lambda V_{DS}) & \text{for } 0 < V_{DS} \le (V_{GD} - V_{TE}) \end{cases}$$

where:

l = channel length modulation, measured in 1volts

$V_{TE}$ = threshold voltage, in volts

$V_{TO}$ = zero-bias threshold voltage, in volts

$\gamma$= bulk-threshold parameter, in volts

j = surface potential at strong inversion, in volts

$V_{BS}$ = bulk-to-source voltage, in volts

$V_{BD}$ = bulk-drain voltage, in volts

$V_{DS}$ = drain-to-source voltage, in volts

## 4.7.4 Time-Domain Model

The time-domain model takes into account the charge-storage effects of the junction diodes used to model MOSFETs. The diodes are modeled using the diode time-domain model described in the Diodes Parts Bin chapter.

## 4.7.5 AC Small-Signal Model

In the linearized small-signal model, the junction diodes used to model the MOSFETs are replaced by their equivalent small-signal models.

$C_{GB}$, $C_{GS}$, $C_{GD}$ are zero-bias junction capacitances.

$$g_m = \frac{dI_D}{dV_{GS}}\Big|_{OP} \qquad g_{BS} = \frac{dI_{BS}}{dV_{BS}}\Big|_{OP}$$

$$g_{DS} = \frac{dI_D}{dV_{GS}}\Big|_{OP} \qquad g_{BD} = \frac{dI_{BD}}{dV_{BD}}\Big|_{OP}$$

$$g_{mBS} = \frac{dI_D}{dV_{BS}}\Big|_{OP}$$

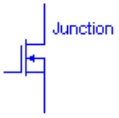
## 4.7.6 MOSFET Level 1 Model Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| VTO | Threshold voltage | 0 | V |
| KP | Transconductance coefficient | 2e-05 | $A/V^2$ |
| LAMBDA | Channel-length modulation | 0 | 1/V |
| PHI | Surface potential | 0.6 | V |
| GAMMA | Bulk-threshold parameter | 0 | V**0.5 |
| RD | Drain ohmic resistance | 0 | W |
| RS | Source ohmic resistance | 0 | W |
| IS | Bulk-junction saturation current | 1e-14 | A |
| CGBO | Gate-bulk overlap capacitance per meter channel length | 0 | F |
| CGDO | Gate-drain overlap capacitance per meter channel length | 0 | F |

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| CGSO | Gate-source overlap capacitance per meter channel width | 0 | F |
| CBD | Zero-bias bulk-drain junction capacitance | 0 | F |
| CBS | Zero-bias bulk-source junction capacitance | 0 | F |
| PB | Bulk-junction potential | 0.8 | V |
| RSH | Drain and source diffusion sheet resistance | 0 | W |
| CJ | Zero-bias bulk junction bottom capacitance per m2 of junction area | 0 | $F/m^2$ |
| MJ | Bulk junction bottom grading coefficient | 0.5 | – |
| CJSW | Zero-bias bulk junction sidewall capacitance per m of junction perimeter. | 0 | F/m |
| MJSW | Bulk junction sidewall grading coefficient | 0.5 | – |
| JS | Bulk junction saturation current per m2 of junction area | 0 | $A/m^2$ |
| TOX | Oxide thickness | 1e-07 | m |
| NSUB | Substrate doping | 0 | $1/cm^3$ |
| NSS | Surface state density | 0 | $1/cm^2$ |
| TPG | Type of gate material | 1 | – |
| LD | Lateral diffusion | 0 | m |
| UO | Surface mobility | 600 | $cm^2/Vs$ |
| KF | Flicker noise coefficient | 0 | – |
| AF | Flicker noise exponent | 1 | – |
| FC | Coefficient for forward-bias depletion capacitance formula | 0.5 | – |
| TNOM | Parameter measurement temperature | 27 | °C |

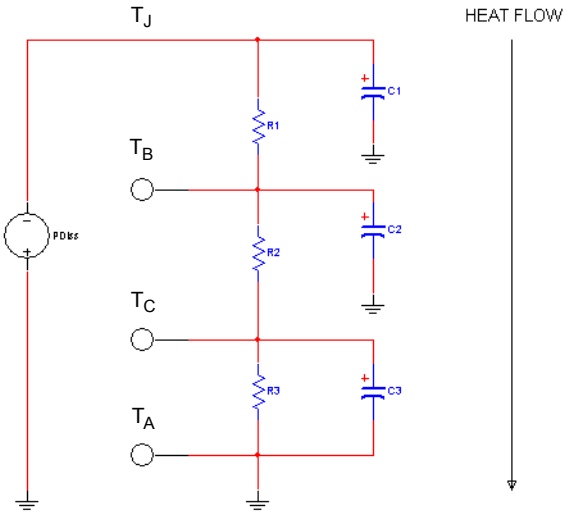
$r_D = r_S$ = 10% to 15% of the on-state drain-source resistance, $R_{DS(on)}$.

# 4.8 MOSFET Thermal Model




This is an interactive device that lets you simulate the heat generated in a MOSFET. Pressing "T" on your keyboard lets you toggle the displayed parameter between Junction, Dielectric Bond and Case.

The following thermal electrical equivalent circuit represents the device's model.

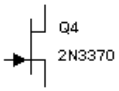



Heat generated in a device's junction flows from a higher temperature region through each resistor-capacitor pair to a lower temperature region.

PDiss is a current source; its amplitude is the power consumed by the MOSFET. The voltages of the nodes $T_J$, $T_B$, $T_C$ and $T_A$ represent the temperature rise of the junction point of the MOSFET, dielectric bond of the MOSFET, case of the MOSFET and ambient temperature.

The ambient temperature is considered constant (no temperature rise), so the voltage of $T_A$ is zero and $T_A$ is grounded.

# 4.9 JFETs (Junction FETs)




The JFET is a unipolar, voltage-controlled transistor that uses an induced electrical field to control current. The current through the transistor is controlled by the gate voltage. The more negative the voltage, the smaller the current.

A JFET consists of a length of an n-type or p-type doped semiconductor material called a channel. The ends of the channel are called the source and the drain. The terminal with the arrowhead represents the gate.

In an n-channel JFET, the gate consists of p-type material surrounding the n-channel. In a p-channel JFET, the gate consists of n-type material surrounding the p-channel.

## 4.9.1 DC Model

The DC model characteristic is determined by a nonlinear current source, $I_D$.

Forward characteristics ($V_{DS} \geq 0$):

$$I_D = \begin{cases} 0 & \text{for } (V_{GS} - V_{TO}) \leq 0 \\ -\beta(V_{GS} - V_{TO})^2(1 + \lambda V_{DS}) & \text{for } 0 < (V_{GS} - V_{TO}) \leq V_{DS} \\ \beta(V_{DS}[2(V_{GS} - V_{TO}) - V_{DS}](1 + \lambda V_{DS}) & \text{for } 0 < V_{DS} \leq (V_{GS} - V_{TO}) \end{cases}$$

Reverse characteristics ($V_{DS} < 0$):

$$I_D = \begin{cases} 0 & \text{for } (V_{GS} - V_{TO}) \leq 0 \\ -\beta(V_{GS} - V_{TO})^2(1 + \lambda V_{DS}) & \text{for } 0 < (V_{GS} - V_{TO}) \leq V_{DS} \\ \beta(V_{DS}[2(V_{GS} - V_{TO}) - V_{DS}](1 + \lambda V_{DS}) & \text{for } 0 < V_{DS} \leq (V_{GS} - V_{TO}) \end{cases}$$

where:

$V_{GS}$ = gate-source voltage, in volts

$V_{DS}$ = drain-source voltage, in volts

$V_{GD}$ = gate-drain voltage, in volts

$V_{GS(off)}$ = gate-source cutoff voltage, in volts

$I_S$ = saturation current for the gate-drain and gate-source diode junctions

$I_D$ = drain-to-source current, in amperes

$I_{DSS}$ = drain-to-source saturation current, in amperes

$\beta = \frac{I_{DSS}}{\left[V_{GS(off)}\right]^2}$ = transconductance parameter in $A/V^2$

l = channel-length modulation parameter measured in 1/V

Other symbols used in these equations are defined in "JFET Model Parameters and Defaults".

***Note*** β is not to be confused with $g_m$, the AC small-signal gain mentioned later in this chapter.

The charge storage occurring in the two gate junctions is modeled by the diode time-domain model described in the Diodes Parts Bin chapter.

The diodes used to model the JFETs are represented by their small-signal models.

$$g_m = \frac{dI_D}{dV_{GS}}\Big|_{OP}$$

$$g_{DS} = \frac{dI_D}{dV_{DS}}\Big|_{OP}$$

$$g_{GS} = \frac{dI_{GS}}{dV_{GS}}\Big|_{OP}$$

$$g_{GD} = \frac{dI_{GD}}{dV_{GD}}\Big|_{OP}$$

where

$g_m$ = AC small-signal gain

$g_{DS}$ = small-signal forward admittance or transconductance

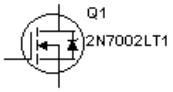
$g_{GS}$ and $g_{GD}$ are normally very small because the diode junctions are not forward-biased. $I_{GS}$ and $I_{GD}$ are the diode current expressions mentioned in the diode modeling section.

## 4.9.2 JFET Model Parameters and Defaults

| Symbol | Parameter Name | Default | Example | Unit |
|---|---|---|---|---|
| VTO | Threshold voltage | -2 | -2 | V |
| BETA | Transconductance coefficient | 0.0001 | 1e-03 | A/V |
| LAMBDA | Channel-length modulation | 0 | 1e-04 | $1/V^2$ |
| RD | Drain ohmic resistance | 0 | 100 | W |
| RS | Source ohmic resistance | 0 | 100 | W |
| IS | Gate-junction saturation current | 1e-14 | 1e-14 | A |
| Cgd | Zero-bias gate-drain junction capacitance | 0 | 1e-12 | F |
| Cgs | Zero-bias gate-source junction capacitance | 0 | 5e-12 | F |
| PB | Gate-junction potential | 1 | .06 | V |
| B | Doping tail parameter | 1 | 1.1 | - |
| KF | Flicker noise coefficient | 0 | - | - |
| AF | Flicker noise exponent | 1 | - | - |
| FC | Coefficient for forward-bias depletion capacitance formula | .5 | - | - |
| TNOM | Parameter measurement temperature | 27 | 50 | °C |

$r_D = r_S$ = 10% to 15% of the on-state drain-to-source resistance, $R_{DS(on)}$.

# 4.10 Power MOSFET (N/P)




The double-diffused or DMOS transistor is an example of a power MOSFET. This device is fabricated on a lightly doped *n*-type substrate with a heavily doped region at the bottom for drain contact. Two diffusions are used, one to create the *p*-type body region and another to create the *n*-type source region.

The DMOS device is operated by applying a positive gate voltage, $v_{GS}$, greater than the threshold voltage $V_t$, which induces a lateral *n* channel in the *p*-type body region underneath the gate oxide. Current is conducted through the resulting short channel to the substrate and then vertically down the substrate to the drain.

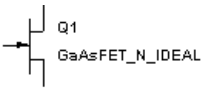
The DMOS transistor can have a breakdown voltage as high as 600 V and a current capability as high as 50 A is possible.

Power MOSFETs have threshold voltages in the range of 2 to 4 V. In comparison with BJTs, power MOSFETs do not suffer second breakdown, nor do they require the large base-drive currents of power BJTS. They also have a higher speed of operation than the power BJTs. These advantages make power MOSFETs suited to switching applications, such as in motor-control circuits.

# 4.11 Power MOSFET Complementary

These DMOS dual N- and P-channel enhancement mode power field effect transistors minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

# 4.12 N-Channel & P-Channel GaAsFET




This component is a high-speed field-effect transistor that uses gallium arsenide (GaAs) as the semiconductor material rather than silicon. It is generally used as a very high frequency amplifier (into the gigahertz range). A GaAsFET consists of a length of n-type or p-type doped GaAs called the channel. The ends of the channel are called the source and the drain. The terminal with the arrowhead represents the gate. GaAsFETs are used in microwave applications.

## 4.12.1 Model and Characteristic Equations

The GaAsFET component is based on the Statz model.

$$Id = \begin{cases} 0 \quad \text{for } V_{gs} - V_{TO} < 0 \\ \beta * \left(1 + \lambda * \mathrm{V_{ds}}\right) * \left(V_{gs} - V_{TO}\right)^2 * \dfrac{\left(1 - \left(1 - V_{ds} * \dfrac{\alpha}{3}\right)^3\right)}{1 + \beta * \left(V_{gs} - V_{TO}\right)} \quad \text{for } \mathrm{V_{gs}} - \mathrm{V_{TO}} \geq 0 \end{cases}$$

where:

$V_{gs}$ = gate-source voltage

$V_{ds}$ = drain-source voltage

$V_{TO}$ = threshold voltage; equivalent to the gate-source cutoff voltage

a = saturation voltage

b = transconductance

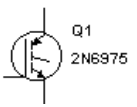
l = channel-length modulation

*Id* = drain to source current

## 4.12.2 GaAsFET Parameters and Defaults

| Symbol | Parameter name | Default | Unit |
|---|---|---|---|
| VTO | Pinch-off voltage | -2 | V |
| BETA | Transconductance | 0.0001 | $A/V^2$ |
| B | Doping tail extending parameter | 0.3 | 1/V |
| ALPHA | Saturation voltage | 2 | 1/V |
| LAMBDA | Channel-length modulation | 0 | 1/V |
| RD | Drain ohmic resistance | 0 | W |
| RS | Source ohmic resistance | 0 | W |
| CGS | Zero-bias G-S junction capacitance | 0 | F |
| CGD | Zero-bias G-D junction capacitance | 0 | F |
| PB | Gate junction potential | 1 | V |
| KF | Flicker noise coefficient | 0 | - |
| AF | Flicker noise exponent | 1 | - |
| FC | Coefficient for forward-bias depletion capacitance formula | 0.5 | |

# 4.13 IGBT




The IGBT is an MOS gate-controlled power switch with a very low on-resistance. It is similar in structure to the MOS-gated thyristor, but maintains gate control of the anode current over a wide range of operating conditions.

The low on-resistance feature of the IGBT is due to conductivity modulation of the n epitaxial layer grown on a $p^+$ substrate. The on-resistance values have been reduced by a factor of

about 10 compared with those of conventional n-channel power MOSFETs of similar size and voltage capability.

Changes to the epitaxial structure and the addition of recombination centers are responsible for the reduction in the fall time and an increase in the latching current level of the IGBT. Fall times as low as 0.1µs and latching currents as high as 50A can be achieved, while retaining on-resistance values <0.2Ω for a 0.09cm$^2$ chip area.

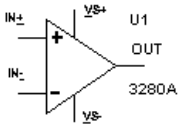
# 4.14 Unijunction Transistors




The Programmable Unijunction Transistor is designed for adjustable characteristics such as valley current, peak current and intrinsic standoff ratio.

# Chapter 5
# Analog Components

## 5.1 Opamp




An ideal operational amplifier (Opamp) is an amplifier with infinite gain, infinite input impedance and zero output impedance. With the application of negative feedback, Opamps can be used to implement functions such as addition, subtraction, differentiation, integration, averaging and amplification.

An opamp can have a single input and single output, a differential input and single output, or a differential input and differential output.

### 5.1.1 Ideal Opamp Model

The ideal opamp model is the fastest to simulate. Its characteristics include:

- open-loop voltage gain (A)

  The open-loop gain is the gain of the opamp without any feedback applied which in the ideal opamp is infinite. This is not possible in the typical opamp, but it will be in the order of 120 dB.

- frequency response

  The frequency response of an opamp is finite and its gain decreases with frequency. For stability, a dominant pole is intentionally added to the opamp to control this decreasing gain with frequency. In an internally compensated opamp, the response typically is set for -6dB/octive roll off with a -3dB frequency in range of 10 Hz. With an externally

compensated Opamps, the -3 dB corner frequency can be changed by adding an external capacitor.

- unity-gain bandwidth

  This is the frequency at which the gain of the opamp is equal to 1. This is the highest frequency at which the opamp can be used, typically as a unity gain buffer.

- common mode rejection ratio (CMRR)

  This is the ability of an opamp to reject or to not amplify a signal that is applied to both its input pins expressed as a ratio (in dBs) of its common mode gain to its open loop gain.

- slew rate

  This is the rate of change of output voltage expressed in volts per microsecond.

## 5.1.2 Opamp: Background Information

The operational amplifier is a high-gain block based upon the principle of a differential amplifier. It is common to applications dealing with very small input signals.

The open-loop voltage gain (A) is typically very large (10e+5 to 10e+6). If a differential input is applied across the “+” and “-” terminals, the output voltage will be:

V = A * (V+ - V-)

The differential input must be kept small, since the opamp saturates for larger signals. The output voltage will not exceed the value of the positive and negative power supplies (Vp), also called the rails, which vary typically from 5 V to 15 V. This property is used in a Schmitt trigger, which sets off an alarm when a signal exceeds a certain value.

Other properties of the opamp include a high input resistance (Ri) and a very small output resistance (Ro). Large input resistance is important so that the opamp does not place a load on the input signal source. Due to this characteristic, opamps are often used as front-end buffers to isolate circuitry from critical signal sources.

Opamps are also used in feedback circuits, comparators, integrators, differentiators, summers, oscillators and wave-shapers. With the correct combination of resistors, both inverting and non-inverting amplifiers of any desired voltage gain can be constructed.

## 5.1.3 Opamp: Simulation Models

Several types of simulation models are included in Multisim. The following model levels are used to distinguish between the various models:

- Virtual 3T — this is the simplest model with the opamp modeled as a gain block with a differential input and a single ended output.
- Virtual 5T — this is a more complex model in which the supply voltages are included in the simulation.
- Real — these are models of increasing complexity where additional control pins are supported.

### 5.1.3.1 Virtual 3-Terminal Opamp

This is the simplest simulation model.

The modeled opamp parameters are:

- open loop gain
- input resistance
- output resistance
- negative voltage swing
- positive voltage swing
- input offset voltage
- slew rate
- unity-gain bandwidth
- input bias current
- input offset current
- compensation capacitance

The opamp is modeled by distributing the open-loop voltage gain, *A,* across three stages. The first and second stages model the first and second poles of the opamp, and the third stage models the output impedance.

The same model is used for DC, time-domain and AC analyses.

$$I_{B1} = I_{BIAS} + \frac{I_{OS}}{2}$$

$$I_{B2} = I_{BIAS} - \frac{I_{OS}}{2}$$

$$I_1 = \frac{A_1 * V_{IN1}}{R_1}$$

$$A_1 = A^{1/3}$$

where

| | | |
|---|---|---|
| $A_1$ | = | open-loop voltage gain of the first stage |
| $R_{IN}$ | = | input resistance, in ohm |
| $I_{BIAS}$ | = | input bias current, in amperes |
| $I_{OS}$ | = | input offset current, in amperes |

$$R_1 = 1\ \text{k}\Omega$$

$$f_{P1} = \frac{f_u}{A}$$

$$C_1 = \frac{1}{2\pi * R_1 * f_{P1}}$$

The slew rate limits the rate of change of $I_1$ to model the rate of change of output voltage.

$$I_1 = \frac{A_2 * V_{IN_2}}{R_2}$$

$$A_2 = A^{1/3}$$

$$R_2 = R_{OUT}$$

where

| | | |
|---|---|---|
| $R_{OUT}$ | = | output resistance |

A third stage is introduced by specifying the location of the second pole:

$$C_2 = \frac{1}{2\pi * R_2 * f_{P2}}$$

$$R_2 = 1\ \text{k}\Omega$$

$$R_3 = R_{OUT}$$

$$I_3 = \frac{A^{1/3} * V_{IN}}{R_3}$$

where

| | | |
|---|---|---|
| $f_u$ | = | unity-gain bandwidth in hertz; i.e., the frequency at which the open-loop voltage gain equals 1. |
| $f_{P2}$ | = | second-pole frequency. A third stage may be introduced by specifying the location of a second pole in hertz. |
| $C_C$ | = | compensation capacitance, which shifts the dominant pole to the left in the frequency response. Its value is typically 30-40 picofarads. |
| *SR* | = | slew rate, which is the rate of change of output voltage (in V/s) in response to a step input. |

## 5.1.3.2 Virtual 5-Terminal Opamp

This is a more complex simulation model that takes into account the supply voltages of the opamp. This model is a differential input, single output model based on the Boyle-Cohn-Pederson macro model, which includes the supply voltage connections. This model supports second order effects such as common-mode rejection, output voltage and current limiting characteristics of the opamp in addition to the first order effects.

The modeled opamp parameters are:

- open loop gain
- input resistance
- output resistance
- slew rate
- unity-gain bandwidth

- common mode rejection (CMRR)
- input bias current
- input offset current
- input bias current
- input offset voltage
- input bias voltage
- output voltage swing
- output current limiting

The internal components of a 741 opamp are shown below.

The circuit is divided into three stages. The input stage consists of ideal transistors, Q1 and Q2, and associated sources and passive elements. It produces the linear and nonlinear differential mode (DM) and common mode (CM) input characteristics. The capacitor, $C_{e,}$ introduces a second order-effect for the slew rate and C1 introduces a second-order effect to the phase response.

$$I_{C1} = \frac{SR * C_C}{2}$$

$$C_e = \frac{2 * I_C}{SR} \qquad R_{C1} = \frac{1}{2\pi * f_u * C_C}$$

$$I_{B1} = I_{bs} + \frac{I_{OS}}{2}$$

$$\beta_1 = \frac{I_{C1}}{I_{B1}}$$

$$\beta_2 = \frac{I_{C1}}{I_{B2}}$$

$$I_{EE}\left(\frac{(\beta_1 + 1)}{\beta_1} + \frac{(\beta_2 + 1)}{\beta_2}\right) I_{C1}$$

$$R_E = \frac{200}{I_{EE}}$$

Assume $I_{S1 = 1e-16}$

$$I_{S2} = I_{S1}\left(1 + \frac{V_{OS}}{0.025}\right)$$

$$C_1 = \frac{C_C}{2}\tan\Delta\varphi$$

The interstage provides the DM and CM gains and consists of voltage-controlled current sources $g_{cm,}$ $g_a$ and $g_b$ and resistors, $R_{02}$ and $R_{2.}$ The dominant time constant of the opamp is provided by the internal feed-back capacitor, $c_{c.}$ In some opamps, the two nodes of $c_c$ are made available to the outside world for external compensation. The output stage models DC and AC output resistance. The elements *d3*, *vc*, *d4* and ve provide maximum desired voltage swings. Elements *d1*, *d2*, *rcc* and *gc* provide the current-limiting function.

## Interstage:

$$g_m = \frac{I_C}{0.02585}$$

$$R_{e1} = \frac{\beta_{1+}\beta_{2}}{\beta_{1+}\beta_{2+2}}\left[R_{C1} - \frac{1}{g_m}\right]$$

$$g_a = \frac{1}{R_{C1}}$$

$$g_b = \frac{AR_C}{100e^3 R_{02}}$$

$$G_{cm} = \frac{G_a}{C_{MRR}}$$

### Output stage:

$$I_x = 2 * I_c g_b - I_{SC}$$

$$I_{SD} = I_x \exp\left(\frac{-R_{01} * I_{SC}}{0.025}\right)$$

$$R_{CC} = \frac{0.025}{100 i_x} \ln \frac{I_x}{I_{SD}}$$

$$G_C = \frac{1}{R_C}$$

$$V_C = V_{CC} - V_{SW}^{+} + V_T * I_n \frac{I_{SC}}{I_{SD}}$$

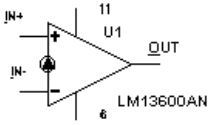
$$V_E = V_{ee} - V_{SW}^{-} + V_T * I_n \frac{I_{SC}}{I_{SD}}$$

### 5.1.3.3 Real Models

Models are supplied by various manufacturers of real-world opamps. Some are simple three- or five-terminal models, while others have additional pins to support functions such as external compensation and output offset balance controls.

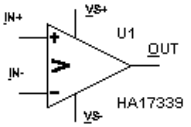
Each model is unique as it was developed by the individual companies to support their products. Therefore, a general description of each model is not possible.

# 5.2 Norton Opamp




The Norton amplifier, or the current-differencing amplifier (CDA) is a current-based device. Its behavior is similar to an opamp, but it acts as a transresistance amplifier where the output voltage is proportional to the input current.

# 5.3 Comparator




A comparator is an IC operational-amplifier whose halves are well balanced and without hysteresis and is therefore suitable for circuits in which two electrical quantities are compared. The comparator components may model conversion speed, quantization error, offset error and output current limitation.

A comparator is a circuit that compares two input voltages and produces an output in either of two states, indicating the greater than or less than relationship of the inputs.

A comparator switches to one state when the input reaches the upper trigger point. It switches back to the other state when the input falls below the lower trigger point.

A voltage comparator may be implemented with any op-amp, with consideration for operating frequencies and slew rate, or with specialized ICs such as the LM339.

The comparator compares a reference voltage, fixed or variable, with an input waveform.

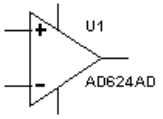
If the input is applied to the non-inverting input and the reference to the inverting input (lower circuit), the comparator will be operating in the non-inverting mode. In this case, when the input voltage is equal to (or slightly less than) the reference voltage the output will be at its lowest limit (near the negative supply) and when the input is equal to (or slightly greater than) the reference voltage the output will change to its highest value (near the positive supply).

If the inverting and non-inverting terminals are reversed (upper circuit) the comparator will operate in the inverting mode.

## 5.3.1 Comparator: Simulation models

A virtual comparator is provided along with several levels of simulation models of increasing complexity and accuracy. Similar to the opamps, the real models are developed by the manufacturers and may have additional pins to model added functions.

# 5.4 Wide Band Amplifier




The typical opamp, such as a general purpose 741 type opamp, has been internally compensated for a unity gain bandwidth of about 1 MHz. Wide band amplifiers are opamps that have been designed with a unity gain bandwidth of greater than 10 MHz and typically in the 100 MHz range. These devices are used for application such as video amplifiers.

## 5.4.1 Wide Band Amplifier: Simulation models

The same levels of simulation model as the opamps are provided with several levels of simulation models of increasing complexity and accuracy.

The following model levels are used to distinguish between these models:

- L1 - this is the simplest model with the opamp modeled as a gain block with a differential input and a single ended output.
- L2 - this is a more complex model in which the supply voltages are included in the simulation.
- L3 - this is a model of increasing complexity where additional control pins are supported.
- L4 - this is the most complex and accurate model with a majority of the external control pins modeled.

# 5.5 Special Function

These are a group of analog devices that are used for the following applications:

- instrumentation amplifier
- video amplifier
- multiplier/divider
- preamplifier
- active filter
- high precision reference

## 5.5.1 Special Function: Simulation models

The same levels of simulation model as the opamps are provided with several levels of simulation models of increasing complexity and accuracy.

The following model levels are used to distinguish between these models:

- L1 - this is the simplest model with the opamp modeled as a gain block with a differential input and a single ended output.
- L2 - this is a more complex model in which the supply voltages are included in the simulation.
- L3 - this is a model of increasing complexity where additional control pins are supported.
- L4 - this is the most complex and accurate model with a majority of the external control pins modeled.

# Chapter 6
# TTL

## 6.1 Standard TTL




The characteristics of the standard TTL series can be illustrated by the 7400 quad NAND gate IC.

The 74 series uses a nominal supply voltage ($V_{OC}$) of 5V and can operate reliably over the range 4.75 to 5.25 V. The voltages applied to any input of a standard 74 series IC must never exceed +5.5 V. The maximum negative voltage that can be applied to a TTL input is -0.5 V.

The 74 series IC is designed to operate in ambient temperatures ranging from 0 to 70° C. The guaranteed worst-case DC noise margins for the 74 series are 400 mV.

A standard TTL NAND gate requires an average power of 10 mV.

A standard TTL output can typically drive 10 standard TTL inputs.

## 6.2 Schottky TTL

The basic circuitry of the standard TTL series forms the central part of several other TTL series, including the Schottky TTL, 74S series.

The Schottky TTL (the 74S series) reduces the storage-time delay by not allowing the transistor to go as deeply into saturation. The 74S series does this by using a Schottky barrier diode connected between the base and the collector of each transistor.

Circuits in the 74S series also use smaller resistor values to help improve switching times. This increases the circuit average power dissipation to about 20 mW. These circuits also use a Darlington pair to provide a shorter output rise time when switching from ON to OFF.

# 6.3 Low-Power Schottky TTL

The low-power Schottky TTL (the 74LS series) is lower in power and slower in speed than the 74S series. It uses the Schottky-clamped transistor, but with larger resistor values than the 74S series. The larger resistor values reduce the power requirements of the circuit, but increase the switching times.

A NAND gate in the 74LS series typically has an average propagation delay of 9.5 ns and an average power dissipation of 2 mW.

# 6.4 74xx

## 6.4.1 74xx00 (Quad 2-In NAND)

This device contains four independent 2-input NAND gates.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 6.4.2 74xx01 (Quad 2-In NAND)

This device contains four independent 2-input NAND gates.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 6.4.3 74xx02 (Quad 2-In NOR)

This device contains four independent 2-input NOR gates.

Logic function:

$Y = \overline{A+B}$

NOR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

## 6.4.4 74xx03 (Quad 2-In NAND (Ls-OC))

This device contains four independent 2-input NAND gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## 6.4.5 74xx04 (Hex INVERTER)

This device contains six independent INVERTER gates.

Logic function:

$Y = \overline{A}$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 6.4.6 74xx05 (Hex INVERTER (OC))

This device contains six independent INVERTER gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{A}$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 6.4.7 74xx06 (Hex INVERTER (OC))

This device contains six independent INVERTER gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{A}$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 6.4.8 74xx07 (Hex BUFFER (OC))

This device contains six independent BUFFER/non-inverting gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{A}$

BUFFER gate truth table:

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

## 6.4.9 74xx08 (Quad 2-In AND)

This device contains four independent 2-input AND gates.

Logic function:

$Y = AB$

AND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## 6.4.10 74xx09 (Quad 2-In AND (OC))

This device contains four independent 2-input AND gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = AB$

AND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## 6.4.11 74xx10 (Tri 3-In NAND)

This device contains three independent 3-input NAND gates.

Logic function:

$Y = \overline{ABC}$

NAND gate truth table

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 |

## 6.4.12 74xx100 (8-Bit Bist Latch)

The 74100 is an 8-bit bistable latch.

8-bit bistable latch truth table:

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| D | G | Q | $\overline{Q}$ |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| X | 0 | Q0 | $\overline{Q0}$ |

## 6.4.13 74xx107 (Dual JK FF(clr))

This device is a positive pulse-triggered flip-flop. It contains two independent J-K flip-flops with individual J-K, clock, and direct clear inputs.

JK flip-flop truth table:

| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
|---|---|---|---|---|---|
| 0 | X | X | X | 0 | 1 |
| 1 | · | 0 | 0 | Hold | |
| 1 | · | 1 | 0 | 1 | 0 |
| 1 | · | 0 | 1 | 0 | 1 |
| 1 | · | 1 | 1 | Toggle | |

## 6.4.14 74xx109 (Dual JK FF (+edge, pre, clr))

This device contains two independent J-K positive edge-triggered flip-flops.

JK flip-flop truth table:

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | $Q_0$ | $\overline{Q}_0$ |

† The output levels are not guaranteed to meet the minimum levels for $V_{OH}$. Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

## 6.4.15 74xx11 (Tri 3-In AND)

This device contains three independent 3-input AND gates.

Logic function:

Y = ABC

AND gate truth table:

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |

## 6.4.16 74xx112 (Dual JK FF(-edge, pre, clr))

This device contains two independent J-K negative edge-triggered flip-flops.

JK flip-flop truth table:

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

† The output levels in this configuration are not guaranteed to meet the minimum levels for $V_{OH}$. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

## 6.4.17 74xx113 (Dual JK MS-SLV FF (-edge, pre))

This device contains two independent J-K negative edge-triggered flip-flops.

JK flip-flop truth table:

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| PR | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | H | L |
| H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | Toggle | |
| H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

$Q_0$ = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

## 6.4.18 74xx114 (Dual JK FF (-edge, pre, com clk & clr))

This device contains two independent J-K negative edge-triggered flip-flops.

JK flip-flop truth table:

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

† The output levels in this configuration are not guaranteed to meet the minimum levels for $V_{OH}$ if the lows at preset and clear are near $V_{IL}$ minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

## 6.4.19 74xx116 (Dual 4-bit latches (clr))

This device contains two independent 4-bit latches. Each 4-bit latch has an independent asynchronous clear input and a gated two-input enable circuit.

Sample 4-bit latch truth table:

| | INPUTS | | | OUTPUT |
|---|---|---|---|---|
| | ENABLE | | | |
| $\overline{CLR}$ | C1 | C2 | DATA | Q |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | X | 1 | X | Hold |
| 1 | 1 | X | X | Hold |
| 0 | X | X | X | 0 |

## 6.4.20 74xx12 (Tri 3-In NAND (OC))

This device contains three independent 3-input NAND gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{ABC}$

NAND gate truth table:

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 |

## 6.4.21 74xx125 (Quad bus BUFFER w/3-state Out)

This device contains four independent BUFFER/non-inverting gates with 3-state outputs.

BUFFER gate truth table:

| $\overline{A}$ | G | Y |
|---|---|---|
| 1 | 0 | 0 |
| 0 | 0 | 1 |
| X | 1 | Z |

Z = high impedance

The output of the bus buffer is disabled when G is high.

## 6.4.22 74xx126 (Quad bus BUFFER w/3-state Out)

This device contains four independent BUFFER/non-inverting gates with 3-state outputs.

BUFFER gate truth table

| A | G | Y |
|---|---|---|
| 1 | 1 | 1 |
| 0 | 1 | 0 |
| X | 0 | Z |

Z = high impedance

The output of the bus buffer is disabled when G is low.

## 6.4.23 74xx13 (Dual 4-In NAND (Schmitt))

This device is a dual 4-input Schmitt-triggered NAND gate.

## 6.4.24 74xx132 (Quad 2-In NAND (Schmitt))

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 1 | 1 | 0 |
| 0 | X | 1 |
| X | 0 | 1 |

VT+ = 1.8V (at 5 Volt test condition)
VT- = 0.95V (at 5 Volt test condition)

## 6.4.25 74xx133 (13-In NAND)

Logic function:

$Y = \overline{ABCDEFGHIJKLM}$

NAND gate truth table

| INPUTS A THRU M | Y |
|---|---|
| All inputs 1 | 0 |
| One or more inputs 0 | 1 |

## 6.4.26 74xx134 (12-In NAND w/3-state Out)

12-Input NAND with 3-state outputs:

| INPUTS A THRU L | OC | Y |
|---|---|---|
| All inputs 1 | 0 | 0 |
| One or more inputs 0 | 0 | 1 |
| Don't care | 1 | Z |

Z = high impedance (off)

## 6.4.27 74xx135 (Quad Ex-OR/NOR Gate)

This device can operate as Exclusive-OR gate (C input low) or as Exclusive-NOR gate (C input high).

Exclusive-OR/NOR gate truth table:

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

## 6.4.28 74xx136 (Quad 2-in Exc-OR gate)

This device is a quadruple 2-input exclusive-OR gate with open-collector outputs.

Exclusive-OR gate truth table:

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## 6.4.29 74xx138 (3-to-8 Dec)

This device decodes one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs.

3-to-8 decoder/demultiplexer truth table:

| | | | SELECT | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{GL}$ | G1 | $\overline{G2}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | 1 | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | X | X | X | Output corresponding to stored address 0; all others 1 | | | | | | | |

## 6.4.30 74xx139 (Dual 2-to-4 Dec/DEMUX)

This decoder/demultiplexer contains two individual two-line to four-line decoders. It features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

2-to-4 decoder/demultiplexer truth table:

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| ENABLE | SELECT | | | | | |
| $\overline{G}$ | B | A | Y0 | Y1 | Y2 | Y3 |
| 1 | X | X | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |

## 6.4.31 74xx14 (Hex INVERTER (Schmitt))

A key feature of this integrated circuit is its high noise immunity. Due the to the Schmitt-trigger action, this device is ideal for circuits that are susceptible to unwanted small signals, such as noise.

INVERTER gate truth table:

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

The voltage threshold levels are as follows:

VT- = 0.95V (at 5 Volt test condition)
VT+ = 1.8V (at 5 Volt test condition)

## 6.4.32 74xx145 (BCD-to-Decimal Dec)

The BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers.

BCD to decimal decoder/driver truth table:

| | INPUTS | | | | OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| INVALID | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 6.4.33 74xx147 (10-to-4 Priority Enc)

This TTL encoder features priority decoding of the inputs to ensure that only the highest-order data line is encoded. It encodes nine data lines to four-line (8-4-2-1) BCD.

10l-line to 4-line priority encoder truth table:

| INPUTS | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | D | C | B | A |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | 0 | 1 | 1 | 0 |
| X | X | X | X | X | X | X | 0 | 1 | 0 | 1 | 1 | 1 |
| X | X | X | X | X | X | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| X | X | X | X | X | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| X | X | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| X | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| X | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

## 6.4.34 74xx148 (8-to-3 Priority Enc)

This TTL encoder features priority decoding of the inputs to ensure that only the highest-order data line is encoded. It encodes eight data lines to three-line (4-2-1) binary (octal).

8-line to 3-line priority encoder truth table:

| | INPUTS | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **EI** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **A2** | **A1** | **A0** | **GS** | **EO** |
| 1 | X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | X | X | X | X | X | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | X | X | X | X | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | X | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

## 6.4.35 74xx15 (3 3-Input AND)

Logic function:

$Y = ABC$

AND gate truth table:

| A | B | C | Y |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 0 | X | X | 0 |
| X | 0 | X | 0 |
| X | X | 0 | 0 |

## 6.4.36 74xx150 (1-of-16 Data Sel/MUX)

This device can select one of sixteen data sources when a 4-bit binary number is applied to the inputs. It is equipped with one enable input and a complementary output.

Truth table:

| INPUTS | | | | | OUTPUTS |
|---|---|---|---|---|---|
| **D** | **C** | **B** | **A** | $\overline{\mathbf{G}}$ | **W** |
| X | X | X | X | 1 | $\overline{1}$ |
| 0 | 0 | 0 | 0 | 0 | $\overline{EO}$ |
| 0 | 0 | 0 | 1 | 0 | $\overline{E1}$ |
| 0 | 0 | 1 | 0 | 0 | $\overline{E2}$ |
| 0 | 0 | 1 | 1 | 0 | $\overline{E3}$ |
| 0 | 1 | 0 | 0 | 0 | $\overline{E4}$ |
| 0 | 1 | 0 | 1 | 0 | $\overline{E5}$ |
| 0 | 1 | 1 | 0 | 0 | $\overline{E6}$ |
| 0 | 1 | 1 | 1 | 0 | $\overline{E7}$ |
| 1 | 0 | 0 | 0 | 0 | $\overline{E8}$ |
| 1 | 0 | 0 | 1 | 0 | $\overline{E9}$ |
| 1 | 0 | 1 | 0 | 0 | $\overline{E10}$ |
| 1 | 0 | 1 | 1 | 0 | $\overline{E11}$ |
| 1 | 1 | 0 | 0 | 0 | $\overline{E12}$ |
| 1 | 1 | 0 | 1 | 0 | $\overline{E13}$ |
| 1 | 1 | 1 | 0 | 0 | $\overline{E14}$ |
| 1 | 1 | 1 | 1 | 1 | $\overline{E15}$ |

## 6.4.37 74xx151 (1-of-8 Data Sel/MUX)

This data selector/multiplexer contains full on-chip binary decoding to select the desired data source. It selects one of eight data sources and is equipped with one enable input and two complementary outputs.

Data selector/multiplexer truth table:

| SELECT | | | STROBE | OUTPUTS | |
|---|---|---|---|---|---|
| **C** | **B** | **A** | $\overline{\mathbf{G}}$ | **Y** | **W** |
| X | X | X | 1 | 0 | $\overline{1}$ |
| 0 | 0 | 0 | 0 | D0 | $\overline{D0}$ |
| 0 | 0 | 1 | 0 | D1 | $\overline{D1}$ |
| 0 | 1 | 0 | 0 | D2 | $\overline{D2}$ |
| 0 | 1 | 1 | 0 | D3 | $\overline{D3}$ |
| 1 | 0 | 0 | 0 | D4 | $\overline{D4}$ |
| 1 | 0 | 1 | 0 | D5 | $\overline{D5}$ |
| 1 | 1 | 0 | 0 | D6 | $\overline{D6}$ |
| 1 | 1 | 1 | 0 | D7 | $\overline{D7}$ |

## 6.4.38 74xx152 (Data Sel/MUX)

This data selector/multiplexer contains full on-chip binary decoding to select one-of-eight data sources.

Data selector/multiplexer truth table:

| SELECT INPUTS | | | OUTPUT |
|---|---|---|---|
| C | B | A | W |
| 0 | 0 | 0 | $\overline{D0}$ |
| 0 | 0 | 1 | $\overline{D1}$ |
| 0 | 1 | 0 | $\overline{D2}$ |
| 0 | 1 | 1 | $\overline{D3}$ |
| 1 | 0 | 0 | $\overline{D4}$ |
| 1 | 0 | 1 | $\overline{D5}$ |
| 1 | 1 | 0 | $\overline{D6}$ |
| 1 | 1 | 1 | $\overline{D7}$ |

## 6.4.39 74xx153 (Dual 4-to-1 Data Sel/MUX)

This data selector/multiplexor contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

Data selector/multiplexer truth table:

| SELECT | | DATA INPUTS | | | | STROBE | OUTPUTS |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | $\overline{G}$ | Y |
| X | X | X | X | X | X | 1 | 0 |
| 0 | 0 | 0 | X | X | X | 0 | 0 |
| 0 | 0 | 1 | X | X | X | 0 | 1 |
| 0 | 1 | X | 0 | X | X | 0 | 0 |
| 0 | 1 | X | 1 | X | X | 0 | 1 |
| 1 | 0 | X | X | 0 | X | 0 | 0 |
| 1 | 0 | X | X | 1 | X | 0 | 1 |
| 1 | 1 | X | X | X | 0 | 0 | 0 |
| 1 | 1 | X | X | X | 1 | 0 | 1 |

# 6.4.40 74xx154 (4-to-16 Dec/DEMUX)

This 4-line-to-16-line decoder uses TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs are low.

4-to-16 decoder/demultiplexer truth table:

| INPUTS | | | | | | OUTPUTS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{G1}$ | $\overline{G2}$ | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## 6.4.41 74xx155 (Dual 2-to-4 Dec/DEMUX)

This device features a dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address inputs.

Decoder/demultiplexer truth table:

| SELECT | | STROBE | DATA | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| A | B | $\overline{G}$ | C | Y0 | Y1 | Y2 | Y3 |
| X | X | 1 | X | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| X | X | X | 0 | 1 | 1 | 1 | 1 |

## 6.4.42 74xx156 (Dual 2-to-4 Dec/DEMUX (OC))

This device contains two 2-to-4 decoders/demultiplexers.

Decoder/demultiplexer truth table:

| SELECT | | STROBE | DATA | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| A | B | $\overline{G}$ | C | Y0 | Y1 | Y2 | Y3 |
| X | X | 1 | X | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| X | X | X | 0 | 1 | 1 | 1 | 1 |

## 6.4.43 74xx157 (Quad 2-to-1 Data Sel/MUX)

This device contains inverters and drivers to supply full on-chip data selection to the four output gates. It presents true data.

A 4-bit word is selected from one of two sources and is routed to the four outputs.

Data selector/multiplexer truth table:

| STROBE | SELECT | | | OUTPUTS |
|---|---|---|---|---|
| $\overline{G}$ | $\overline{A}$/B | A | B | Y |
| 1 | X | X | X | 0 |
| 0 | 0 | 0 | X | 0 |
| 0 | 0 | 1 | X | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 1 | X | 1 | 1 |

## 6.4.44 74xx158 (Quad 2-to-1 Data Sel/MUX)

This device contains inverters and drivers to supply full on-chip data selection to the four output gates. It presents inverted data to minimize propagation delay time.

A 4-bit word is selected from one of two sources and is routed to the four outputs.

Data selector/multiplexer truth table:

| STROBE | SELECT | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | $\overline{A}$/B | A | B | Y |
| 1 | X | X | X | 1 |
| 0 | 0 | 0 | X | 1 |
| 0 | 0 | 1 | X | 0 |
| 0 | 1 | X | 0 | 1 |
| 0 | 1 | X | 1 | 0 |

## 6.4.45 74xx159 (4-to-16 Dec/DEMUX (OC))

This 4-line-to-16-line decoder uses TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive open-collector outputs when both the strobe inputs are low.

The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low.

Decoder/demultiplexer truth table:

| INPUTS | | | | | | OUTPUTS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{G1}$ | $\overline{G2}$ | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## 6.4.46 74xx16 (Hex INVERTER (OC))

This device contains six inverters. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{A}$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

# 6.4.47 74xx160 (Sync 4-bit Decade Counter (clr))

This synchronous, presettable decade counter features an internal carry look-ahead for fast counting.

Sample decade counter truth table:

| INPUTS | | | | | | OUTPUTS | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|
| $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | DN | QN | TC | |
| 0 | X | X | X | X | X | 0 | 0 | Reset (clear) |
| 1 | · | X | X | l | l | 0 | 0 | |
| 1 | · | X | X | l | h | 1 | (1) | Parallel load |
| 1 | · | h | h | h | X | count | (1) | Count |
| 1 | X | l | X | h | X | $q_n$ | (1) | Hold (do nothing) |
| 1 | X | X | l | h | X | $q_n$ | 0 | |

| | | |
|---|---|---|
| 1 | = | High voltage level |
| h | = | High voltage level one setup prior to the low-to-high clock transition |
| 0 | = | Low voltage level |
| l | = | Low voltage level one setup prior to the low-to-high clock transition |
| $q_n$ | = | Lower case letters indicate the state of the referenced output prior to the low-to-high clock transition |
| X | = | Don't care |
| · | = | Low-to-high clock transition |
| (1) | = | The TC output is High when CET is High and the counter is at Terminal Count (HLLH) |

# 6.4.48 74xx161 (Sync 4-bit Bin Counter)

This synchronous, presettable binary counter features an internal carry look-ahead for fast counting.

Sample 4-bit bin counter truth table:

| INPUTS | | | | | | OUTPUTS | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|
| $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | DN | QN | TC | |
| 0 | X | X | X | X | X | 0 | 0 | Reset (clear) |
| 1 | · | X | X | l | l | 0 | 0 | |
| 1 | · | X | X | l | h | 1 | (1) | Parallel load |
| 1 | · | h | h | h | X | count | (1) | Count |
| 1 | X | l | X | h | X | $q_n$ | (1) | Hold (do |
| 1 | X | X | l | h | X | $q_n$ | 0 | nothing) |

| | | |
|---|---|---|
| 1 | = | High voltage level |
| h | = | High voltage level one setup prior to the low-to-high clock transition |
| 0 | = | Low voltage level |
| l | = | Low voltage level one setup prior to the low-to-high clock transition |
| $q_n$ | = | Lower case letters indicate the state of the referenced output prior to the low-to-high clock transition |
| X | = | Don't care |
| · | = | Low-to-high clock transition |
| (1) | = | The TC output is High when CET is High and the counter is at Terminal Count (HHHH) |

## 6.4.49 74xx162 (Sync 4-bit Decade Counter)

This synchronous, presettable decade counter features an internal carry look-ahead for fast counting.

Sample decade counter truth table:

| INPUTS | | | | | | OUTPUTS | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|
| $\overline{SR}$ | CP | CEP | CET | $\overline{PE}$ | DN | QN | TC | |
| l | · | X | X | X | X | 0 | 0 | Reset (clear) |
| h | · | X | X | l | l | 0 | 0 | |
| h | · | X | X | l | h | 1 | (2) | Parallel load |
| h | · | h | h | h | X | count | (2) | Count |
| h | X | l | X | h | X | $q_n$ | (2) | Hold (do nothing) |
| h | X | X | l | h | X | $q_n$ | 0 | |

| | | |
|---|---|---|
| 1 | = | High voltage level |
| h | = | High voltage level one setup prior to the low-to-high clock transition |
| 0 | = | Low voltage level |
| l | = | Low voltage level one setup prior to the low-to-high clock transition |
| $q_n$ | = | Lower case letters indicate the state of the referenced output prior to the low-to-high clock transition |
| X | = | Don’t care |
| · | = | Low-to-high clock transition |
| (2) | = | The TC output is High when CET is High and the counter is at Terminal Count (HLLH) |

## 6.4.50 74xx163 (Sync 4-bit Binary Counter)

This synchronous, presettable, 4-bit binary counter features an internal carry look-ahead for fast counting.

# 6.4.51 74xx164 (8-bit Parallel-Out Serial Shift Reg)

This 8-bit shift register has gated serial inputs and an asynchronous clear.

Shift register truth table:

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| $\overline{CLEAR}$ | CLOCK | A | B | $Q_A$ | $Q_B$ | ... | $Q_H$ |
| L | X | X | X | L | L | | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | | $Q_{Gn}$ |

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Gn}$ = the level of $Q_A$ or $Q_G$ before the most-recent ↑ transition of the clock; indicates a one-bit shift.

# 6.4.52 74xx165 (Parallel-load 8-bit Shift Reg)

This serial shift-register shifts the data in the direction of QA toward QH when clocked. To load the data at the 8-inputs into the device, apply a low level at the shift/load input. This register is equipped with a complementary output at the eighth bit.

Shift register truth table:

| INPUTS | | | | | | | | INTERNAL O/P | | OUTPUTS |
|---|---|---|---|---|---|---|---|---|---|---|
| SHIFT/ LOAD | CLK INH | CLK | SERIAL | PARALLEL A | B | C | D | $\overline{QA}$ | QB | QH |
| 0 | X | X | X | a | b | c | d | a | b | h |
| 1 | 0 | 0 | X | X | X | X | X | QA0 | QB0 | QH0 |
| 1 | 0 | · | 1 | X | X | X | X | 1 | QAn | QGn |
| 1 | 0 | · | 0 | X | X | X | X | 0 | QAn | QGn |
| 1 | 1 | X | X | X | X | X | X | QA0 | QB0 | QH0 |

· = transition from low to high

a,b,c,d = the level of steady state input at A, B, C, or D respectively

# 6.4.53 74xx166 (Parallel-load 8-bit Shift Reg)

This shift-register is a parallel-in or serial-in, serial out device. It shifts the data in the direction of QA toward QH when clocked. It features an active-low clear input. To load the data at the 8-inputs into the device, apply a low level at the shift/load input.

Shift register truth table:

| INPUTS | | | | | | | | | INTERNAL O/P | | OUTPUTS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CLR | SHIFT/ LOAD | CLK INH | CLK | SERIAL | PARALLEL A through H | | | | $\overline{QA}$ | $\overline{QB}$ | QH |
| 0 | X | X | X | X | X | X | X | X | 0 | 0 | 0 |
| 1 | X | 0 | 0 | X | X | X | X | X | QA0 | QB0 | QH0 |
| 1 | 0 | 0 | · | X | A TO H | | | | a | b | 1 |
| 1 | 1 | 0 | · | 1 | X | X | X | X | 1 | QAn | QGn |
| 1 | 1 | 0 | · | 0 | X | X | X | X | 0 | QAn | QGn |
| 1 | X | 1 | · | X | X | X | X | X | QA0 | QB0 | QH0 |

· = transition from low to high

a,b,c,d = the level of steady state input at A, B, C, or D respectively

# 6.4.54 74xx169 (Sync 4-bit up/down Binary Counter)

This synchronous presettable 4-bit binary counter has an internal carry look-ahead for cascading in high speed counting applications.

Up/down counter truth table:

| $\overline{ENP}$ | $\overline{ENT}$ | D/U | $\overline{CLK}$ | LOAD | A | $\overline{B}$ | $\overline{C}$ | D | QA | QB | QC | QD | RCO |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | X | 0 | X | X | X | X | A | B | C | D | 1* |
| 0 | 0 | 1 | · | 1 | X | X | X | X | Count Down | | | | 1* |
| 0 | 0 | 0 | · | 1 | X | X | X | X | Count Up | | | | 1* |
| 1 | X | X | X | X | X | X | X | X | Qa0 | Qb0 | Qc0 | Qd0 | 1* |
| X | 1 | X | X | X | X | X | X | X | Qa0 | Qb0 | Qc0 | Qd0 | 1* |

1* = during the UP count RCO goes LOW at count 15.
during the DOWN count RCO goes LOW at count 0.

## 6.4.55 74xx17 (Hex BUFFER (OC))

This device contains six independent BUFFER/Drivers. For correct performance, the open collector outputs require pull-up resistors.

BUFFER gate truth table:

| $\overline{A}$ | Y |
|---|---|
| $\overline{0}$ | 0 |
| $\overline{1}$ | 1 |

## 6.4.56 74xx173 (4-bit D-type Reg w/3-state Out)

D-type register truth table:

| | | DATA ENABLE | | DATA | OUTPUT |
|---|---|---|---|---|---|
| CLEAR | CLK | $\overline{G1}$ | $\overline{G2}$ | D | Q |
| 1 | X | X | X | X | 0 |
| 0 | 0 | X | X | X | Q0 |
| 0 | · | 1 | X | X | Q0 |
| 0 | · | X | 1 | X | Q0 |
| 0 | · | 0 | 0 | 0 | 0 |
| 0 | · | 0 | 0 | 1 | 1 |

## 6.4.57 74xx174 (Hex D-type FF (clr))

D-type flip-flop truth table:

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| CLEAR | CLOCK | D | Q | $\overline{Q}$† |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
$Q_0$ = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

## 6.4.58 74xx175 (Quad D-type FF (clr))

D-type flip-flop truth table:

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| CLEAR | CLOCK | D | Q | $\overline{Q}$† |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
$Q_0$ = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

## 6.4.59 74xx180 (9-bit Odd/even Par GEN)

This 9-bit (8 data bits plus 1 parity bit) parity generator/checker features odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications.

Parity generator/checker truth table:

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| S OF H's AT A THRU H | EVEN | ODD | S EVEN | S ODD |
| Even | 1 | 0 | 1 | 0 |
| Odd | 1 | 0 | 0 | 1 |
| Even | 0 | 1 | 0 | 1 |
| Odd | 0 | 1 | 1 | 0 |
| X | 1 | 1 | 0 | 0 |
| X | 0 | 0 | 1 | 1 |

# 6.4.60 74xx181 (Alu/Function Generator)

ALU/function generator truth table:

**ACTIVE - LOW DATA**

| SELECTION | | | | M=H | M=L; ARITHMETIC OPERATIONS | |
|---|---|---|---|---|---|---|
| S3 | S2 | S1 | S0 | LOGIC FUNCTIONS | Cn=L (NO CARRY) | Cn=H (WITH CARRY) |
| 0 | 0 | 0 | 0 | F=$\overline{A}$ | F= A MINUS 1 | F= A |
| 0 | 0 | 0 | 1 | F= $\overline{AB}$ | F= AB MINUS 1 | F= AB |
| 0 | 0 | 1 | 0 | F= $\overline{A+B}$ | F= A$\overline{B}$ MINUS 1 | F= A$\overline{B}$ |
| 0 | 0 | 1 | 1 | F= 1 | F= MINUS 1(2's comp) | F= Zero |
| 0 | 1 | 0 | 0 | F= $\overline{A+B}$ | F= A PLUS (A+$\overline{B}$) | F= A PLUS(A+$\overline{B}$) Plus 1 |
| 0 | 1 | 0 | 1 | F= $\overline{B}$ | F= AB PLUS(A+$\overline{B}$) | F= AB PLUS (A+B) PLUS 1 |
| 0 | 1 | 1 | 0 | F= $\overline{A\text{“+”}B}$ | F= A MINUS B MINUS 1 | F= A MINUS |
| 0 | 1 | 1 | 1 | F= A+$\overline{B}$ | F= A+$\overline{B}$ | F= (A+$\overline{B}$)PLUS1 |
| 1 | 0 | 0 | 0 | F= $\overline{A}$B | F= A PLUS (A+B) | F= A PLUS (A+B) PLUS 1 |
| 1 | 0 | 0 | 1 | F= $\overline{A\text{“+”}B}$ | F= A PLUS B | F= A PLUS B PLUS |
| 1 | 0 | 1 | 0 | F= B | F= A$\overline{B}$ PLUS(A+B) | F= AB PLUS (A+B) PLUS 1 |
| 1 | 0 | 1 | 1 | F= A + B | F= (A + B) | F= (A+B) PLUS 1 |

# 6.4.61 74xx182 (Look-ahead Carry GEN)

The high-speed, look-ahead carry generator can anticipate a carry across four binary adders or groups of adders. It is cascadable to perform full look-ahead across n-bit adders.

Truth table for $\overline{G}$ output:

| INPUTS | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|
| $\overline{G3}$ | $\overline{G2}$ | $\overline{G1}$ | $\overline{G0}$ | $\overline{P3}$ | $\overline{P2}$ | $\overline{P1}$ | $\overline{G}$ |
| 0 | X | X | X | X | X | X | 0 |
| X | 0 | X | X | 0 | X | X | 0 |
| X | X | 0 | X | 0 | 0 | X | 0 |
| X | X | X | 0 | 0 | 0 | 0 | 0 |
| All other combinations | | | | | | | 1 |

Truth table for $\overline{P}$ output:

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{P3}$ | $\overline{P2}$ | $\overline{P1}$ | $\overline{P0}$ | $\overline{P}$ |
| 0 | 0 | 0 | 0 | 0 |
| All other combinations | | | | 1 |

Truth table for $\overline{Cn+x}$ output:

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{G0}$ | $\overline{P0}$ | Cn | $\overline{Cn+x}$ |
| 0 | X | X | 1 |
| X | 0 | 1 | 1 |
| All other combinations | | | 0 |

Truth table for $\overline{Cn+y}$ output:

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{G1}$ | $\overline{G0}$ | $\overline{P1}$ | $\overline{P0}$ | Cn | $\overline{Cn+y}$ |
| 0 | X | X | X | X | 1 |
| X | 0 | 0 | X | X | 1 |
| X | X | 0 | 0 | 1 | 1 |
| All other combinations | | | | | 0 |

Truth table for $\overline{Cn+z}$ output:

| INPUTS | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|
| $\overline{G2}$ | $\overline{G1}$ | $\overline{G0}$ | $\overline{P2}$ | $\overline{P1}$ | $\overline{P0}$ | Cn | $\overline{Cn+z}$ |
| 0 | X | X | X | X | X | X | 1 |
| X | 0 | X | 0 | X | X | X | 1 |
| X | X | 0 | 0 | 0 | X | X | 1 |
| X | X | X | 0 | 0 | 0 | 1 | 1 |
| All other combinations | | | | | | | 0 |

1 = High level
0 = Low level
X = Don’t care

# 6.4.62 74xx190 (Sync BCD up/down Counter)

This device is a synchronous, BCD, reversible up/down counter.

Counter TC and $\overline{RC}$ truth table:

| INPUTS | | | TERMINAL COUNT STATE | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| $\overline{U}$/D | $\overline{CE}$ | CP | Q0 | Q1 | Q2 | Q3 | TC | $\overline{RC}$ |
| 1 | 1 | X | 1 | X | X | 1 | 0 | 1 |
| 0 | 1 | X | 1 | X | X | 1 | 1 | 1 |
| 0 | 0 | | 1 | X | X | 1 | 1 | |
| 0 | 1 | X | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | X | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | | 0 | 0 | 0 | 0 | 1 | |

1 = High voltage level
0 = Low voltage level
X = Don’t care
= Low pulse

## 6.4.63 74xx191 (Sync 4-bit up/down Counter)

This device is a synchronous, 4-bit binary, reversible up/down counter.

Counter TC and $\overline{\text{RC}}$ truth table:

| INPUTS | | | TERMINAL COUNT STATE | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| $\overline{\text{U}}$/D | $\overline{\text{CE}}$ | CP | Q0 | Q1 | Q2 | Q3 | TC | $\overline{\text{RC}}$ |
| 1 | 1 | X | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | X | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | | 1 | 1 | 1 | 1 | 1 | |
| 0 | 1 | X | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | X | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | | 0 | 0 | 0 | 0 | 1 | |

1 = High voltage level
0 = Low voltage level
X = Don’t care
= Low pulse

## 6.4.64 74xx192 (Sync BCD Up/down Counter)

This device is a synchronous, BCD, reversible up/down counter.

Sample up/down counter truth table:

| INPUTS | | | | | | | | OUTPUTS | | | | | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MR | $\overline{PL}$ | CPU | CPD | D0 | D1 | D2 | D3 | Q0 | Q1 | Q2 | Q3 | $\overline{TCU}$ | $\overline{TCD}$ | |
| 1 | X | X | 0 | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 0 | Reset |
| 1 | X | X | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Parallel load |
| 0 | 0 | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | 0 | X | 1 | X | X | 1 | Qn=Dn | | | | 0 | 1 | |
| 0 | 0 | 1 | X | 1 | X | X | 1 | Qn=Dn | | | | 1 | 1 | |
| 0 | 1 | · | 1 | X | X | X | X | Count up | | | | $1^1$ | 1 | Count up |
| 0 | 1 | 1 | · | X | X | X | X | Count down | | | | 1 | $1^2$ | Count down |

· = transition from low to high
$1^1$ = $\overline{TC}U$=CPU at terminal count up (HLLH)
$1^2$ = $\overline{TC}D$=CPD at terminal count down (LLLL)

# 6.4.65 74xx193 (Sync 4-bit Bin Up/down Counter)

This device is a synchronous, 4-bit binary, reversible up/down counter.

Sample up/down counter truth table:

| INPUTS | | | | | | | | OUTPUTS | | | | | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MR | $\overline{PL}$ | CPU | CPD | D0 | D1 | D2 | D3 | Q0 | Q1 | Q2 | Q3 | $\overline{TCU}$ | $\overline{TCD}$ | |
| 1 | X | X | 0 | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 0 | Reset |
| 1 | X | X | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Parallel load |
| 0 | 0 | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | 0 | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | |
| 0 | 0 | 1 | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 0 | 1 | · | 1 | X | X | X | X | Count up | | | | $1^1$ | 1 | Count up |
| 0 | 1 | 1 | · | X | X | X | X | Count down | | | | 1 | $1^2$ | Count down |

· = transition from low to high
$1^1$ = $\overline{TC}U$=CPU at terminal count up (HHHH)
$1^2$ = $\overline{TC}D$=CPD at terminal count down (LLLL)

# 6.4.66 74xx194 (4-bit Bidirect Univ. Shift Reg)

This bidirectional shift register has parallel-inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line.

Shift register truth table:

| | MODE | | | SERIAL | | PARALLEL | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{\text{CLEAR}}$ | S1 | S0 | CLK | LEFT | RIGHT | A | B | C | D | QA | QB | QC | QD |
| 0 | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 |
| 1 | X | X | 0 | X | X | X | X | X | X | QA0 | QB0 | QC0 | QD0 |
| 1 | 1 | 1 | · | X | X | a | b | c | d | a | b | c | d |
| 1 | 0 | 1 | · | X | 1 | X | X | X | X | 1 | QAn | QBn | QCn |
| 1 | 0 | 1 | · | X | 0 | X | X | X | X | 0 | QAn | QBn | QCn |
| 1 | 1 | 0 | · | 1 | X | X | X | X | X | QBn | QCn | QDn | 1 |
| 1 | 1 | 0 | · | 0 | X | X | X | X | X | QBn | QCn | QDn | 0 |
| 1 | 0 | 0 | X | X | X | X | X | X | X | QA0 | QB0 | QC0 | QD0 |

| | | |
|---|---|---|
| · | = | transition from low to high |
| a, b, c, d | = | the level of steady state input at inputs A, B, C, or D respectively |
| QA0, QB0, QC0, QD0 | = | the level of QA, QB, QC, or QD, respectively, before the indicated steady state input conditions were established |
| QAn, QBn, QCn, QDn | = | the level of QA, QB, QC, or QD before the most recent negative transition of the clock |

# 6.4.67 74xx195 (4-bit Parallel-Access Shift Reg)

This 4-bit register has parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear.

Shift register truth table:

| | | | SERIAL | | PARALLEL | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CLEAR** | **SHIFT/ LOAD** | **CLK** | **J** | **$\overline{K}$** | **A** | **B** | **C** | **D** | **QA** | **QB** | **QC** | **QD** | **$\overline{QD}$** |
| 0 | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | · | X | X | a | b | c | d | a | b | c | d | $\overline{d}$ |
| 1 | 1 | 0 | X | X | X | X | X | X | QA0 | QB0 | QC0 | QD0 | $\overline{QD0}$ |
| 1 | 1 | · | 0 | 1 | X | X | X | X | QA0 | QA0 | QBn | QCn | $\overline{QCn}$ |
| 1 | 1 | · | 0 | 0 | X | X | X | X | 0 | QAn | QBn | QCn | $\overline{QCn}$ |
| 1 | 1 | · | 1 | 1 | X | X | X | X | 1 | QAn | QBn | QCn | $\overline{QCn}$ |
| 1 | 1 | · | 1 | 0 | X | X | X | X | $\overline{QA}$n | QAn | QBn | QCn | $\overline{QCn}$ |

| | | |
|---|---|---|
| · | = | transition from low to high |
| a, b, c, d | = | the level of steady state input at inputs A, B, C, or D respectively |
| QA0, QB0, QC0, QD0 | = | the level of QA, QB, QC, or QD, respectively, before the indicated steady state input conditions were established |
| QAn, QBn, QCn | = | the level of QA, QB, QC before the most recent negative transition of the clock |

# 6.4.68 74xx198 (8-bit Shift Reg (shl/shr ctrl))

This bidirectional register has parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line.

Shift register truth table:

| | MODE | | | SERIAL | | PARALLEL | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **$\overline{CLEAR}$** | **S1** | **S0** | **CLK** | **LEFT** | **RIGHT** | **A ... h** | **QA** | **QB ... QG** | | **QH** |
| 0 | X | X | X | X | X | X | 0 | 0 | 0 | 0 |
| 1 | X | X | 0 | X | X | X | QA0 | QB0 | QG0 | QH0 |
| 1 | 1 | 1 | · | X | X | a...h | a | b | g | h |
| 1 | 0 | 1 | · | X | 1 | X | 1 | QAn | QFn | QGn |
| 1 | 0 | 1 | · | X | 0 | X | 0 | QAn | QFn | QGn |
| 1 | 1 | 0 | · | 1 | X | X | QBn | QCn | QHn | 1 |
| 1 | 1 | 0 | · | 0 | X | X | QBn | QCn | QHn | 1 |
| 1 | 0 | 0 | X | X | X | X | QA0 | QB0 | QG0 | QH0 |

| | | |
|---|---|---|
| · | = | transition from low to high |
| a ... h | = | the level of steady state input at inputs A through H respectively |
| QA0, QB0, QG0, QH0 | = | the level of QA, QB, QG, or QH, respectively, before the indicated steady state input conditions were established |
| QAn, QBn, etc. | = | the level of QA, QB etc., respectively, before the most recent negative transition of the clock |

# 6.4.69 74xx199 (8-bit Shift Reg (sh/ld ctrl))

This device contains an 8-bit shift register with shift/load control.

Shift register truth table:

| MODE | | | | SERIAL | | PARALLEL | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| **CLEAR** | **S/L** | **CLKINH** | **CLK** | **J** | **K** | **A...H** | **QA** | **QB..QG** | **QH** |
| 0 | X | X | X | X | X | X | 0 | 0 | 0 |
| 1 | X | 0 | 0 | X | X | X | QA0 | QB0 | QH0 |
| 1 | 0 | 0 | · | X | X | a...h | a | b..g | h |
| 1 | 1 | 0 | · | 0 | 1 | X | QA0 | QA0 | QGn |
| 1 | 1 | 0 | · | 0 | 0 | X | 0 | QAn | QGn |
| 1 | 1 | 0 | · | 1 | 1 | X | 1 | QCn | 1 |
| 1 | 1 | 0 | · | 1 | 0 | X | $\overline{Q}$An | QAn | QGn |
| 1 | X | 1 | · | X | X | X | QA0 | QB0 | QH0 |

| | | |
|---|---|---|
| · | = | transition from low level to high level |
| a ... h | = | the level of steady state input at inputs A through H respectively |
| QA0, QB0, QG0, QH0 | = | the level of QA, QB, QG, or QH, respectively, before the indicated steady state input conditions were established |
| QAn, QBn, etc. | = | the level of QA, QB etc., respectively, before the most recent negative transition of the clock |

## 6.4.70 74xx20 (Dual 4-In NAND)

This device contains two independent 4-input NAND gates.

Logic function:

$Y = \overline{ABCD}$

NAND gate truth table

| A | B | C | D | Y |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | 1 |
| X | 0 | X | X | 1 |
| X | X | 0 | X | 1 |
| X | X | X | 0 | 1 |

## 6.4.71 74xx21 (Dual 4-In AND)

This device contains two independent 4-input AND gates.

Logic function:

$Y = ABCD$

AND gate truth table:

| A | B | C | D | Y |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 |
| 0 | X | X | X | 0 |
| X | 0 | X | X | 0 |
| X | X | 0 | X | 0 |
| X | X | X | 0 | 0 |

## 6.4.72 74xx22 (Dual 4-In NAND (OC))

This device contains two independent 4-input NAND gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{ABCD}$

NAND gate truth table:

| A | B | C | D | Y |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | 1 |
| X | 0 | X | X | 1 |
| X | X | 0 | X | 1 |
| X | X | X | 0 | 1 |

## 6.4.73 74xx238 (3-to-8 line Dec/DEMUX)

The logic levels at the C B and A inputs select one of the eight lines. G1 is an active-high enable input while G2A and G2B are active-low enable inputs.

3-to-8 decoder/demultiplexer truth table:

| | | | SELECT | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| X | X | 1 | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

## 6.4.74 74xx24 (Dual 4-input NAND Schmitt)

Each circuit in this device functions as a NAND gate or inverter. Due to the Schmitt action, there are different input threshold levels for positive-going and negative-going signals.

## 6.4.75 74xx240 (Octal BUFFER w/3-state Out)

This device has high fan-out, improved fan-in, and 400-mV noise margin.

Octal BUFFER gate truth table:

| $\overline{G}$ | A | Y |
|---|---|---|
| 1 | X | Z |
| 0 | 0 | 1 |
| 0 | 1 | 0 |

Z = High impedance (off)

## 6.4.76 74xx241 (Octal BUFFER w/3-state Out)

This device has high fan-out, improved fan-in, and 400-mV noise margin.

Octal BUFFER gate truth table:

| | INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | A1 | A2 | A3 | A4 | Y1 | Y2 | Y3 | Y4 |
| 1 | X | X | X | X | Z | Z | Z | Z |
| 0 | X | X | X | X | A1 | A2 | A3 | A4 |

Z = High impedance (off)
A1, A2... = The level of the respective input

## 6.4.77 74xx244 (Octal BUFFER w/3-state Out)

This device has high fan-out, improved fan-in, and 400-mV noise margin.

Octal BUFFER gate truth table:

| | INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | A1 | A2 | A3 | A4 | Y1 | Y2 | Y3 | Y4 |
| 1 | X | X | X | X | Z | Z | Z | Z |
| 0 | X | X | X | X | A1 | A2 | A3 | A4 |

Z = High impedance (off)
A1, A2... = The level of the respective input

# 6.4.78 74xx246 (BCD-to-seven segment dec)

The BCD-to-seven-segment decoder/driver features active-low outputs designed for driving indicators directly. It has full ripple-blanking input/output controls and a lamp test input.

BCD-to-seven-segment decoder/driver truth table:

| - | INPUTS | | | | | | BI/ | OUTPUTS | | | | | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N | LT | RBI | D | C | B | A | RBO | a | b | c | d | e | f | g | |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | ON | ON | ON | ON | ON | ON | OFF | |
| | 1 | X | 0 | 0 | 0 | 1 | 1 | OFF | ON | ON | OFF | OFF | OFF | OFF | |
| | 1 | X | 0 | 0 | 1 | 0 | 1 | ON | ON | OFF | ON | ON | OFF | ON | |
| | 1 | X | 0 | 0 | 1 | 1 | 1 | ON | ON | ON | ON | OFF | OFF | ON | |
| | 1 | X | 0 | 1 | 0 | 0 | 1 | OFF | ON | ON | OFF | OFF | ON | ON | |
| | 1 | X | 0 | 1 | 0 | 1 | 1 | ON | OFF | ON | ON | OFF | ON | ON | |
| | 1 | X | 0 | 1 | 1 | 0 | 1 | ON | OFF | ON | ON | ON | ON | ON | |
| | 1 | X | 0 | 1 | 1 | 1 | 1 | ON | ON | ON | OFF | OFF | OFF | OFF | 1 |
| | 1 | X | 1 | 0 | 0 | 0 | 1 | ON | ON | ON | ON | ON | ON | ON | |
| | 1 | X | 1 | 0 | 0 | 1 | 1 | ON | ON | ON | ON | OFF | ON | ON | |
| | 1 | X | 1 | 0 | 1 | 0 | 1 | OFF | OFF | OFF | ON | ON | OFF | ON | |
| | 1 | X | 1 | 0 | 1 | 1 | 1 | OFF | OFF | ON | ON | OFF | OFF | ON | |
| | 1 | X | 1 | 1 | 0 | 0 | 1 | OFF | ON | OFF | OFF | OFF | ON | ON | |
| | 1 | X | 1 | 1 | 0 | 1 | 1 | ON | OFF | OFF | ON | OFF | ON | ON | |
| | 1 | X | 1 | 1 | 1 | 0 | 1 | OFF | OFF | OFF | ON | ON | ON | ON | |
| | 1 | X | 1 | 1 | 1 | 1 | 1 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| | X | X | X | X | X | X | 0 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 2 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 3 |
| | 0 | X | X | X | X | X | 1 | ON | ON | ON | ON | ON | ON | ON | 4 |

Notes:

1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied to the blanking input ($\overline{BI}$), all segment outputs are off regardless of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{BI}$/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

# 6.4.79 74xx247 (BCD-to-seven segment dec)

The BCD -to-seven-segment decoder/driver features active-low outputs designed for driving indicators directly. It has full ripple-blanking input/output controls and a lamp test input.

BCD-to-seven-segment decoder/driver truth table:

| DECIMAL OR FUNCTION | INPUTS | | | | | | BI/ RBO | OUTPUTS | | | | | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | ON | ON | ON | ON | ON | ON | OFF | |
| 1 | 1 | X | 0 | 0 | 0 | 1 | 1 | OFF | ON | ON | OFF | OFF | OFF | OFF | |
| 2 | 1 | X | 0 | 0 | 1 | 0 | 1 | ON | ON | OFF | ON | ON | OFF | ON | |
| 3 | 1 | X | 0 | 0 | 1 | 1 | 1 | ON | ON | ON | ON | OFF | OFF | ON | |
| 4 | 1 | X | 0 | 1 | 0 | 0 | 1 | OFF | ON | ON | OFF | OFF | ON | ON | |
| 5 | 1 | X | 0 | 1 | 0 | 1 | 1 | ON | OFF | ON | ON | OFF | ON | ON | |
| 6 | 1 | X | 0 | 1 | 1 | 0 | 1 | ON | OFF | ON | ON | ON | ON | ON | |
| 7 | 1 | X | 0 | 1 | 1 | 1 | 1 | ON | ON | ON | OFF | OFF | OFF | OFF | 1 |
| 8 | 1 | X | 1 | 0 | 0 | 0 | 1 | ON | ON | ON | ON | ON | ON | ON | |
| 9 | 1 | X | 1 | 0 | 0 | 1 | 1 | ON | ON | ON | ON | OFF | ON | ON | |
| 10 | 1 | X | 1 | 0 | 1 | 0 | 1 | OFF | OFF | OFF | ON | ON | OFF | ON | |
| 11 | 1 | X | 1 | 0 | 1 | 1 | 1 | OFF | OFF | ON | ON | OFF | OFF | ON | |
| 12 | 1 | X | 1 | 1 | 0 | 0 | 1 | OFF | ON | OFF | OFF | OFF | ON | ON | |
| 13 | 1 | X | 1 | 1 | 0 | 1 | 1 | ON | OFF | OFF | ON | OFF | ON | ON | |
| 14 | 1 | X | 1 | 1 | 1 | 0 | 1 | OFF | OFF | OFF | ON | ON | ON | ON | |
| 15 | 1 | X | 1 | 1 | 1 | 1 | 1 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| BI | X | X | X | X | X | X | 0 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 2 |
| RBI | 1 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 3 |
| LT | 0 | X | X | X | X | X | 1 | ON | ON | ON | ON | ON | ON | ON | 4 |

Notes:

1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied to the blanking input ($\overline{BI}$), all segment outputs are off regardless of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{BI}$/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

## 6.4.80 74xx248 (BCD-to-seven segment dec)

The BCD -to-seven-segment decoder/driver features active-high outputs for driving lamp buffers. It has full ripple-blanking input/output controls and a lamp test input.

BCD-to-seven-segment decoder/driver truth table:

| DECIMAL OR FUNCTION | INPUTS | | | | | | BI/ RBO | OUTPUTS | | | | | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 1 | X | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| 3 | 1 | X | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 4 | 1 | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 5 | 1 | X | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 6 | 1 | X | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | |
| 7 | 1 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 8 | 1 | X | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 9 | 1 | X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | |
| 10 | 1 | X | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | |
| 11 | 1 | X | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | |
| 12 | 1 | X | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | |
| 13 | 1 | X | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | |
| 14 | 1 | X | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| 15 | 1 | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| BI | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| RBI | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3 |
| LT | 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4 |

Notes:

1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied to the blanking input ($\overline{BI}$), all segment outputs are low regardless of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{BI}$/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

# 6.4.81 74xx249 (BCD-to-seven segment dec)

The BCD -to-seven-segment decoder/driver features active-high outputs for driving lamp buffers. It has full ripple-blanking input/output controls and a lamp test input.

BCD-to-seven-segment decoder/driver truth table:

| DECIMAL OR FUNCTION | INPUTS | | | | | | BI/RBO | OUTPUTS | | | | | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 1 | X | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| 3 | 1 | X | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 4 | 1 | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 5 | 1 | X | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 6 | 1 | X | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | |
| 7 | 1 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 8 | 1 | X | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 9 | 1 | X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | |
| 10 | 1 | X | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | |
| 11 | 1 | X | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | |
| 12 | 1 | X | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | |
| 13 | 1 | X | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | |
| 14 | 1 | X | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| 15 | 1 | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| BI | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| RBI | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3 |
| LT | 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4 |

Notes:

1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied to the blanking input ($\overline{BI}$), all segment outputs are low regardless of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{BI}$/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

## 6.4.82 74xx25 (Dual 4-In NOR w/Strobe)

This device contains two independent 4-input NOR gates with strobe.

NOR gate with strobe truth table:

| A | B | C | D | G | Y |
|---|---|---|---|---|---|
| 1 | X | X | X | 1 | 0 |
| X | 1 | X | X | 1 | 0 |
| X | X | 1 | X | 1 | 0 |
| X | X | X | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | X | 1 |
| X | X | X | X | 0 | 1 |

## 6.4.83 74xx251 (Data Sel/MUX w/3-state Out)

This device contains full on-chip binary decoding to select one-of-eight data sources and has a strobe-controlled three-state output.

Data selector/multiplexer truth table:

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| SELECT | | | ENABLE | Y | W |
| C | B | A | $\overline{G}$ | | |
| X | X | X | H | Z | Z |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

# 6.4.84 74xx253 (Dual 4-to-1 Data Sel/MUX w/3-state Out)

This Schottky-clamped data selector/multiplexer contains inverters and drivers to supply fully complementary on-chip, binary decoding data selection to the AND-OR gates.

Data selector/multiplexer truth table:

| Select Inputs | | Data Inputs | | | | Output Control | Output |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | $\overline{G}$ | Y |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

Address inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

# 6.4.85 74xx257 (Quad 2-to-1 line Data Sel/MUX)

This device is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. Its 3-state outputs interface directly with the system bus.

Data selector/multiplexer truth table:

| OUTPUT CONTROL | SELECT | A | B | Y |
|---|---|---|---|---|
| 1 | X | X | X | Z |
| 0 | 0 | 0 | X | 0 |
| 0 | 0 | 1 | X | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 1 | X | 1 | 1 |

Z = High impedance (off)

## 6.4.86 74xx258 (Quad 2-to-1 line Data Sel/MUX)

This device is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. Its 3-state outputs interface directly with the system bus.

Data selector/multiplexer truth table:

| OUTPUT CONTROL | SELECT | A | B | Y |
|---|---|---|---|---|
| 1 | X | X | X | Z |
| 0 | 0 | 0 | X | 0 |
| 0 | 0 | 1 | X | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 1 | X | 1 | 1 |

Z = High impedance (off)

## 6.4.87 74xx259 (8-bit Latch)

This 8-bit addressable latch is a 1-of-8 decoder or demultiplexer with active high outputs. It stores single-line data in eight addressable latches.

8-bit addressable latch truth table:

| INPUTS CLEAR | $\overline{G}$ | OUTPUT OF ADDRESSED LATCH | EACH OTHER OUTPUT | FUNCTION |
|---|---|---|---|---|
| 1 | 0 | D | $Q_{i0}$ | Addressable latch |
| 1 | 1 | $Q_{i0}$ | $Q_{i0}$ | Memory |
| 0 | 0 | D | 0 | 8-line demultiplexer |
| 0 | 1 | 0 | 0 | Clear |

## 6.4.88 74xx26 (Quad 2-In NAND (OC))

This device contains four independent 2-input NAND gates.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 1 | 1 | 0 |
| 0 | X | 1 |
| X | 0 | 1 |
| X | X | 1 |
| X | X | 1 |

## 6.4.89 74xx266 (Quad 2-In XNOR (OC))

This device contains four independent 2-input EXCLUSIVE-NOR gates.

Logic function:

$Y = \overline{A} \oplus \overline{B}$

Exclusive-NOR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## 6.4.90 74xx27 (Tri 3-In NOR)

This device contains three independent 3-input NOR gates.

Logic function:

$Y = \overline{A+B+C}$

NOR gate truth table:

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |

## 6.4.91 74xx273 (Octal D-type FF)

D flip-flop truth table

| CLEAR | CLK | D | Q |
|---|---|---|---|
| 0 | X | X | 0 |
| 1 | · | 1 | 1 |
| 1 | · | 0 | 0 |
| 1 | 0 | X | Q0 |

· = transition from low to high

## 6.4.92 74xx279 (Quad SR latches)

The RS flip-flop has an undesired operating condition, where 1 levels at both inputs will cause both outputs to go to a 0 level. This undefined condition must be avoided. Circuits involving feedback will lead to a “race condition” where the output will be unpredictable.

RS flip-flop truth table:

| S | R | Q | $\overline{Q}$ | |
|---|---|---|---|---|
| 0 | 0 | - | - | (no change) |
| 0 | 1 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | X | X | (undefined) |

## 6.4.93 74xx28 (Quad 2-In NOR)

This device contains four independent 2-input NOR gates.

Logic function:

$Y = \overline{A+B}$

NOR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

## 6.4.94 74xx280 (9-bit odd/even parity generator/checker)

9-bit odd/even parity generator/checker truth table:

| NUMBER OF INPUTS A THROUGH I THAT ARE HIGH | Σ - EVEN | Σ- ODD |
|---|---|---|
| 0, 2, 4, 6, 8 | 1 | 0 |
| 1, 3, 5, 7, 9 | 0 | 1 |

Σ = sigma

## 6.4.95 74xx283 (4-bit Bin Full Add)

This device performs the addition of two 4-bit binary numbers. It features full internal look-ahead across all four bits generating the carry term in ten nanoseconds typically.

| Input | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | When C0 = L | | | When C0 = H | | |
| | | | | When C2 = L | | | When C2 = H | | |
| A1 / A3 | B1 / B3 | A2 / A4 | B2 / B4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H = HIGH Level, L = LOW Level

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2.
The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

## 6.4.96 74xx290 (Decade Counter)

This device contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

Decade counter truth table:

| COUNT | QD | QC | QB | QA | R0(1) | R0(2) | R9(1) | R9(2) | QD | QC | QB | QA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | X | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | X | X | 1 | 1 | 1 | 0 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | X | 0 | X | 0 | COUNT | | | |
| 4 | 0 | 1 | 0 | 0 | 0 | X | 0 | X | COUNT | | | |
| 5 | 0 | 1 | 0 | 1 | 0 | X | X | 0 | COUNT | | | |
| 6 | 0 | 1 | 1 | 0 | X | 0 | 0 | X | COUNT | | | |
| 7 | 0 | 1 | 1 | 1 | | | | | | | | |
| 8 | 1 | 0 | 0 | 0 | | | | | | | | |
| 9 | 1 | 0 | 0 | 1 | | | | | | | | |

## 6.4.97 74xx293 (4-bit Binary Counter)

This device contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

Counter truth table:

| RESET IN | | OUTPUT | | | |
|---|---|---|---|---|---|
| $\overline{Ro1}$ | $\overline{Ro2}$ | Qd | Qc | Qb | Qa |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | X | COUNT | | | |
| X | 0 | COUNT | | | |

## 6.4.98 74xx298 (Quad 2-In MUX)

This quadruple two-input multiplexer selects one of two 4-bit data sources and stores data synchronously with system clock.

Multiplexer truth table:

| WORD SELECT | CLK | QA | QB | QC | QD |
|---|---|---|---|---|---|
| 0 | Ø | a1 | b1 | c1 | d1 |
| 1 | Ø | a2 | b2 | c2 | d2 |
| X | Ø | QA0 | QB0 | QC0 | QD0 |

| | | |
|---|---|---|
| , | = | transition from high to low |
| a1, a2, etc. | = | the level of steady state input at A1, A2, etc. |
| QA0, QB0, etc. | = | the level of QA, QB, etc.entered on the most recent negative transition of the clock input |

# 6.4.99 74xx30 (8-In NAND)

Logic function:

$Y = \overline{ABCDEFGH}$

8-input NAND gate truth table:

| INPUTS A THROUGH H | Y |
|---|---|
| All inputs 1 | 0 |
| One or more inputs 0 | 1 |

# 6.4.10074xx32 (Quad 2-In OR)

This device contains four independent 2-input OR gates.

Logic function:

$Y = A+B$

OR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

# 6.4.10174xx33 (Quad 2-In NOR (OC))

This device contains four independent 2-input NOR gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{A+B}$

NOR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

# 6.4.10274xx350 (4-bit Shifter w/3-state Out)

This device shifts 4-bits of data to 0, 1, 2, or 3 places under control of two select lines.

4-bit shifter truth table:

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | S1 | S0 | Y0 | Y1 | Y2 | Y3 |
| 1 | X | X | Z | Z | Z | Z |
| 0 | 0 | 0 | D0 | D1 | D2 | D3 |
| 0 | 0 | 1 | D-1 | D0 | D1 | D2 |
| 0 | 1 | 0 | D-2 | D-1 | D0 | D1 |
| 0 | 1 | 1 | D-3 | D-2 | D-1 | D0 |

Z = High impedance (off)

# 6.4.10374xx351 (Dual Data Sel/MUX w/3-state Out)

The 74351 device is made up of two 8-line-to-1-line data selectors/multiplexors with full decoding on one monolithic chip.

Dual data selector/multiplexor truth table:

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| ENABLE | SELECT | | | | |
| $\overline{G}$ | C | B | A | 1Y | 2Y |
| 1 | X | X | X | Z | Z |
| 0 | 0 | 0 | 0 | $\overline{1D0}$ | $\overline{2D0}$ |
| 0 | 0 | 0 | 1 | $\overline{1D1}$ | $\overline{2D1}$ |
| 0 | 0 | 1 | 0 | $\overline{1D2}$ | $\overline{2D2}$ |
| 0 | 0 | 1 | 1 | $\overline{1D3}$ | $\overline{2D3}$ |
| 0 | X | 0 | 0 | $\overline{D4}$ | $\overline{D4}$ |
| 0 | X | 0 | 1 | $\overline{D5}$ | $\overline{D5}$ |
| 0 | X | 1 | 0 | $\overline{D6}$ | $\overline{D6}$ |
| 0 | X | 1 | 1 | $\overline{D7}$ | $\overline{D7}$ |

# 6.4.10474xx352 (Dual 4-to-1 Data Sel/MUX)

This device contains inverters and drivers to supply fully complementary on-chip, binary decoding data selection to the AND-OR-invert gates.

Data selector/multiplexer truth table:

| SELECT | | DATA INPUTS | | | | | |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | $\overline{G}$ | Y |
| X | X | X | X | X | X | 1 | 1 |
| 0 | 0 | 0 | X | X | X | 0 | 1 |
| 0 | 0 | 1 | X | X | X | 0 | 0 |
| 0 | 1 | X | 0 | X | X | 0 | 1 |
| 0 | 1 | X | 1 | X | X | 0 | 0 |
| 1 | 0 | X | X | 0 | X | 0 | 1 |
| 1 | 0 | X | X | 1 | X | 0 | 0 |
| 1 | 1 | X | X | X | 0 | 0 | 1 |
| 1 | 1 | X | X | X | 1 | 0 | 0 |

# 6.4.10574xx353 (Dual 4-to-1 Data Sel/MUX w/3-state Out)

This device contains inverters and drivers to supply fully complementary on-chip, binary decoding data selection to the AND-OR-invert gates.

Data selector/multiplexer truth table:

| SELECT | | DATA INPUTS | | | | | |
|---|---|---|---|---|---|---|---|
| B | A | C0 | C1 | C2 | C3 | $\overline{G}$ | Y |
| X | X | X | X | X | X | 1 | 1 |
| 0 | 0 | 0 | X | X | X | 0 | 1 |
| 0 | 0 | 1 | X | X | X | 0 | 0 |
| 0 | 1 | X | 0 | X | X | 0 | 1 |
| 0 | 1 | X | 1 | X | X | 0 | 0 |
| 1 | 0 | X | X | 0 | X | 0 | 1 |
| 1 | 0 | X | X | 1 | X | 0 | 0 |
| 1 | 1 | X | X | X | 0 | 0 | 1 |
| 1 | 1 | X | X | X | 1 | 0 | 0 |

# 6.4.10674xx365 (Hex Buffer/Driver w/3-state)

This device features high fan-out, improved fan-in, and can be used to drive terminated lines down to 133 ohms.

Hex buffer/driver truth table:

$Y = A$

| Input | | | Output |
|---|---|---|---|
| $\overline{G1}$ | $\overline{G2}$ | A | Y |
| H | X | X | Hi-Z |
| X | H | X | Hi-Z |
| L | L | H | H |
| L | L | L | L |

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

# 6.4.10774xx366 (Hex Inverter Buffer/Driver w/3-state)

This device is a 3-state Hex inverter buffer/driver.

Sample hex inverter buffer/driver truth table:

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{OE_0}$ | $\overline{OE_1}$ | $I_n$ | $Y_n$ | $\overline{Y}_n$ |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| X | 1 | X | Z | Z |
| 1 | X | X | Z | Z |

1 = High voltage level
0 = Low voltage level
X = Don’t care
Z = High impedance “off” state

# 6.4.10874xx367 (Hex Buffer/Driver w/3-state)

This device features high fan-out, improved fan-in, and can be used to drive terminated lines down to 133 ohms.

Hex buffer/driver truth table:

$Y = A$

| Inputs | | Output |
|---|---|---|
| A | $\overline{G}$ | Y |
| L | L | L |
| H | L | H |
| X | H | Hi-Z |

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

# 6.4.10974xx368 (Hex Inverter Buffer/Driver w/3-state)

This device is a 3-state hex inverter buffer/driver.

Hex inverter buffer/driver truth table:

$Y = \overline{A}$

| Inputs | | Output |
|---|---|---|
| A | $\overline{G}$ | Y |
| L | L | H |
| H | L | L |
| X | H | Hi-Z |

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

## 6.4.110 74xx37 (Quad 2-In NAND)

This device contains four independent 2-input NAND gates.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 6.4.111 74xx373 (Octal D-type Transparent Latches)

This 8-bit register features three-state bus-driving outputs and transparent D-type latches.

D-latch and flip-flop truth table:

| OUTPUT ENABLE | ENABLE LATCH | D | OUTPUT |
|---|---|---|---|
| 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | X | Q0 |
| 1 | X | X | Z |

Z = High impedance (off)

## 6.4.112 74xx374 (Octal D-type FF (+edge))

This 8-bit register features three-state bus-driving outputs and transparent D-type flip-flops.

D-latch and flip-flop truth table:

| OUTPUT ENABLE | ENABLE LATCH | D | OUTPUT |
|---|---|---|---|
| 0 | · | 1 | 1 |
| 0 | · | 0 | 0 |
| 0 | 0 | X | Q0 |
| 1 | X | X | Z |

Z = High impedance (off)
· = Transition from low to high

## 6.4.113 74xx375 (4-bit Bistable Latches)

This device features outputs from a 4-bit latch.

Sample bistable latch truth table:

| D | C | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| X | 0 | Q0 | $\overline{Q0}$ |

## 6.4.114 74xx377 (Octal D-type FF w/en)

This device contains eight flip-flops with single-rail outputs.

Sample D-type flip-flop truth table:

| $\overline{G}$ | CLK | $\overline{DATA}$ | Q | $\overline{Q}$ |
|---|---|---|---|---|
| 1 | X | X | Q0 | $\overline{Q0}$ |
| 0 | · | 1 | 1 | 0 |
| 0 | · | 0 | 0 | 1 |
| X | 0 | X | QO | $\overline{Q0}$ |

## 6.4.115 74xx378 (Hex D-type FF w/en)

This device contains six flip-flops with single-rail outputs.

D-type flip-flop truth table:

| $\overline{G}$ | CLK | $\overline{DATA}$ | Q | $\overline{Q}$ |
|---|---|---|---|---|
| 1 | X | X | Q0 | $\overline{Q0}$ |
| 0 | · | 1 | 1 | 0 |
| 0 | · | 0 | 0 | 1 |
| X | 0 | X | QO | $\overline{Q0}$ |

## 6.4.116 74xx379 (Quad D-type FF w/en)

This device contains four flip-flops with double-rail outputs.

D-type flip-flop truth table:

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{G}$ | CLK | DATA | Q | $\overline{Q}$ |
| 1 | X | X | Q0 | $\overline{Q0}$ |
| 0 | · | 1 | 1 | 0 |
| 0 | · | 0 | 0 | 1 |
| X | 0 | X | Q0 | $\overline{Q0}$ |

## 6.4.117 74xx38 (Quad 2-In NAND (OC))

This device contains four independent 2-input NAND gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 6.4.118 74xx39 (Quad 2-In NAND (OC))

This device contains four independent 2-input NAND gates. For correct performance, the open collector outputs require pull-up resistors.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 6.4.119 74xx390 (Dual Div-by-2, Div-by-5 Counter)

The 74390 device incorporates dual divide-by-two and divide-by-five counters.

BCD count sequence truth table:

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | QD | QC | QB | QA |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |

Notes:

Output QA is connected to input B for BCD count.

Bi-quinary truth table:

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | QA | QD | QC | QB |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 1 | 0 | 0 | 0 |
| 6 | 1 | 0 | 0 | 1 |
| 7 | 1 | 0 | 1 | 0 |
| 8 | 1 | 0 | 1 | 1 |
| 9 | 1 | 1 | 0 | 0 |

Notes:

Output QD is connected to input A for bi-quinary.

# 6.4.12074xx393 (Dual 4-bit Binary Counter)

This device features an independent active-high clear and clock input for each counter. The 74393 is ideal for circuits that require two independent counters.

The 74393 counts from 0 to 15 in binary on every positive transition (low to high) of the clock pulse.

Count sequence truth table:

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | QD | QC | QB | QA |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |

# 6.4.12174xx395 (4-bit Cascadable Shift Reg w/3-state Out)

This device is a 4-bit shift register with 3-state outputs. It features parallel-in and parallel out registers.

4-bit shift register truth table:

| $\overline{OC}$ | $\overline{CLR}$ | $\overline{LD}$/SH | CLK | SER | A | B | C | D | QA | QB | QC | QD | $\overline{QD}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | X | X | X | Z | Z | Z | Z | $\overline{QD}$ |
| 1 | 0 | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | X | X | X | X | X | NO CHANGE | | | | |
| 1 | 1 | 1 | Ø | X | A | B | C | D | QA | QB | QC | QD | QD |
| 1 | 1 | 0 | 1 | X | X | X | X | X | NO CHANGE | | | | |
| 1 | 1 | 0 | Ø | 1 | X | X | X | X | 1 | QA | QB | QC | QC |
| 1 | 1 | 0 | Ø | 0 | X | X | X | X | 0 | QA | QB | QC | QC |

# 6.4.12274xx40 (Dual 4-In NAND)

This device contains two independent 4-input NAND gate.

Logic function:

$Y = \overline{ABCD}$

NAND gate truth table:

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | 1 |
| X | 0 | X | X | 1 |
| X | X | 0 | X | 1 |
| X | X | X | 0 | 1 |

# 6.4.12374xx42 (4-BCD to 10-Decimal Dec)

This BCD-to-decimal decoder consists of eight inverters and ten four-input NAND gates.

4-line to 10-line decimal decoder truth table:

| | BCD INPUT | | | | DECIMAL OUTPUT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **No.** | **D** | **C** | **B** | **A** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INVALID | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 6.4.12474xx43 (Exc-3-to-Decimal Dec)

This excess-3-to-decimal decoder consists of eight inverters and ten four-input NAND gates.

Excess-3-to-decimal decoder truth table

| | EXCESS-3- INPUT | | | | DECIMAL OUTPUT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **No.** | **D** | **C** | **B** | **A** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 6 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 7 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 8 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 9 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INVALID | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 6.4.12574xx44 (Exc-3-Gray-to-Decimal Dec)

This excess-3-gray-to-decimal decoder consists of eight inverters and ten four-input NAND gates.

Excess-3-gray-to-decimal decoder truth table:

| | EXCESS-3-GRAY INPUT | | | | DECIMAL OUTPUT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **No.** | **D** | **C** | **B** | **A** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 6 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 8 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 9 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INVALID | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 6.4.12674425 (Quad Bus Buffer with 3-State)

This bus buffer has 3-state outputs that, when enabled, have the low impedance characteristics of a TTL output and additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pull-up resistors.

# 6.4.12774426 (Quad Bus Buffer with 3-State)

This bus buffer has 3-state outputs that, when enabled, have the low impedance characteristics of a TTL output and additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pull-up resistors.

# 6.4.12874xx445 (BCD-to-Decimal Dec)

This BCD-to-decimal decoder consists of eight inverters and ten four-input NAND gates.

BCD-to-decimal truth table:

| | INPUTS | | | | OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| O | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INVALID | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 6.4.12974xx45 (BCD-to-Decimal Dec)

This BCD-to-decimal decoder consists of eight inverters and ten four-input NAND gates.

BCD-to-decimal truth table:

| | INPUTS | | | | OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INVALID | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 6.4.13074xx46 (BCD-to-seven segment dec)

The 7446 BCD (Binary-Coded Decimal)-to-seven-segment decoder translates a 4-bit BCD input into hexadecimal, and outputs high on the output pins corresponding to the hexadecimal representation of the BCD input. There are provisions for lamp testing and for blanking the outputs.

BCD-to-seven-segment decoder:

| | INPUTS | | | | | | OUTPUTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **No.** | **$\overline{LT}$** | **$\overline{RBI}$** | **D** | **C** | **B** | **A** | **$\overline{BI/RBO}$** | **a** | **b** | **c** | **d** | **e** | **f** | **g** | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| 1 | 1 | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 2 | 1 | X | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| 3 | 1 | X | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 4 | 1 | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 5 | 1 | X | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 6 | 1 | X | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | |
| 7 | 1 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 8 | 1 | X | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 9 | 1 | X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 10 | 1 | X | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | |
| 11 | 1 | X | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | < INVALID |
| 12 | 1 | X | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | |
| 13 | 1 | X | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | < |
| 14 | 1 | X | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| 15 | 1 | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| BI | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| RBI | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| LT | 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

# 6.4.13174xx465 (Octal BUFFER w/3-state Out)

This device has a two-input active-low AND enable gate controlling all eight data buffers.

Octal buffers truth table:

| $\overline{G}1$ | $\overline{G}2$ | A | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | X | Z |
| 0 | 1 | X | Z |
| 1 | 1 | X | Z |

Z = High impedance (off)

# 6.4.13274xx466 (Octal BUFFER w/3-state Out)

This device has a two-input active-low AND enable gate controlling all eight data buffers.

Octal buffers truth table:

| $\overline{G}1$ | $\overline{G}2$ | A | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | X | Z |
| 0 | 1 | X | Z |
| 1 | 1 | X | Z |

Z = High impedance (off)

# 6.4.13374xx47 (BCD-to-seven segment dec)

The 7447 BCD (Binary-Coded Decimal)-to-seven-segment decoder translates a 4-bit BCD input into hexadecimal, and outputs high on the output pins corresponding to the hexadecimal representation of the BCD input. There are provisions for lamp testing and for blanking the outputs.

BCD-to-seven-segment decoder sample truth table:

| Decimal or Function | Inputs | | | | | | | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{LT}$ | $\overline{RBI}$ | A3 | A2 | A1 | A0 | $\overline{BI/RBO}$ | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | L | L | L | L | L | L | H | (Note 2) |
| 1 | H | X | L | L | L | H | H | H | L | L | H | H | H | H | (Note 2) |
| 2 | H | X | L | L | H | L | H | L | L | H | L | L | H | L | |
| 3 | H | X | L | L | H | H | H | L | L | L | L | H | H | L | |
| 4 | H | X | L | H | L | L | H | H | L | L | H | H | L | L | |
| 5 | H | X | L | H | L | H | H | L | H | L | L | H | L | L | |
| 6 | H | X | L | H | H | L | H | H | H | L | L | L | L | L | |
| 7 | H | X | L | H | H | H | H | L | L | L | H | H | H | H | |
| 8 | H | X | H | L | L | L | H | L | L | L | L | L | L | L | |
| 9 | H | X | H | L | L | H | H | L | L | L | H | H | L | L | |
| 10 | H | X | H | L | H | L | H | H | H | H | L | L | H | L | |
| 11 | H | X | H | L | H | H | H | H | H | L | L | H | H | L | |
| 12 | H | X | H | H | L | L | H | H | L | H | H | H | L | L | |
| 13 | H | X | H | H | L | H | H | L | H | H | L | H | L | L | |
| 14 | H | X | H | H | H | L | H | H | H | H | L | L | L | L | |
| 15 | H | X | H | H | H | H | H | H | H | H | H | H | H | H | |
| $\overline{BI}$ | X | X | X | X | X | X | L | H | H | H | H | H | H | H | (Note 3) |
| $\overline{RBI}$ | H | L | L | L | L | L | L | H | H | H | H | H | H | H | (Note 4) |
| $\overline{LT}$ | L | X | X | X | X | X | H | L | L | L | L | L | L | L | (Note 5) |

**Note 2:** $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

**Note 3:** When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

**Note 4:** When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

**Note 5:** When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is OPEN or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

# 6.4.13474xx48 (BCD-to-seven segment dec)

This device features active-high outputs for driving lamp buffers or common-cathode VLEDs. It also has full ripple-blanking input/output controls and a lamp test input.

BCD-to-seven-segment decoder:

| | INPUTS | | | | | | OUTPUTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **No.** | **$\overline{LT}$** | **$\overline{RBI}$** | **D** | **C** | **B** | **A** | **$\overline{BI}$/$\overline{RBO}$** | **a** | **b** | **c** | **d** | **e** | **f** | **g** | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| 1 | 1 | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 2 | 1 | X | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| 3 | 1 | X | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 4 | 1 | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 5 | 1 | X | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 6 | 1 | X | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | |
| 7 | 1 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 8 | 1 | X | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 9 | 1 | X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 10 | 1 | X | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | INVA |
| 11 | 1 | X | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | < LID |
| 12 | 1 | X | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | < |
| 13 | 1 | X | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | < |
| 14 | 1 | X | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| 15 | 1 | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| BI | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| RBI | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| LT | 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

$\overline{BI}$ = active-low blanking input

$\overline{RBI}$ = active-low ripple-blanking input

$\overline{LT}$ = active-low lamp-test input

Notes:

1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied to the blanking input ($\overline{BI}$), all segment outputs are low regardless of any other input level.
3. To place the device in lamp-test mode, $\overline{RBO}$ must be high when $\overline{LT}$ is low. This forces all lamps on.

# 6.4.13574xx51 (AND-OR-INVERTER)

AND-OR INVERTER gate truth table:

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | X | X | 0 | 1 |
| X | 0 | 0 | X | 1 |
| 0 | X | 0 | X | 1 |
| X | 0 | X | 0 | 1 |
| 1 | 1 | X | X | 0 |
| X | X | 1 | 1 | 0 |

# 6.4.13674xx521 (8-Bit Identity Comparitor)

The 74F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input IA=B also serves as an active LOW enable input.

| Inputs | | Output |
|---|---|---|
| $\overline{I}_{A=B}$ | A, B | $\overline{O}_{A=B}$ |
| L | A = B (Note 1) | L |
| L | A ≠ B | H |
| H | A = B (Note 1) | H |
| H | A ≠ B | H |

H = HIGH Voltage Level
L = LOW Voltage Level
**Note 1:** $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

# 6.4.13774xx533 (Octal D-Latch with inverted O/Ps)

| Inputs | | | Output |
|---|---|---|---|
| LE | $\overline{OE}$ | D | $\overline{O}$ |
| H | L | H | L |
| H | L | L | H |
| L | L | X | $\overline{O}_0$ |
| X | H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

# 6.4.13874xx534 (Octal Flip-Flop with inverted Latches)

| Inputs | | | Output |
|---|---|---|---|
| CP | $\overline{OE}$ | D | $\overline{O}$ |
| ⌐↑ | L | H | L |
| ⌐↑ | L | L | H |
| L | L | X | $\overline{O}_0$ |
| X | H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐↑ = LOW-to-HIGH Clock Transition
$\overline{O}_0$ = Value stored from previous clock cycle

# 6.4.13974xx54 (4-wide AND-OR-INVERTER)

4-wide AND-OR-INVERTER truth table:

| INPUTS | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | H | Y |
| 1 | 1 | X | X | X | X | X | X | 0 |
| X | X | 1 | 1 | X | X | X | X | 0 |
| X | X | X | X | 1 | 1 | X | X | 0 |
| X | X | X | X | X | X | 1 | 1 | 0 |
| X | X | X | X | X | X | X | X | 1 |

# 6.4.14074xx55 (2-wide 4-In AND-OR-INVERTER)

AND-OR-INVERTER truth table:

| INPUTS | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | H | Y |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | X | X | X | X | 0 |
| X | X | X | X | 1 | 1 | 1 | 1 | 0 |
| X | X | X | X | X | X | X | X | 1 |

# 6.4.14174xx573 (Octal D-type Latch)

This device contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are in the bi-state mode. When OE is HIGH the

buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | LE | D | O |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $O_0$ |
| H | X | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
$O_0$ = Value stored from previous clock cycle

# 6.4.14274xx574 (Octal D-type Flip-Flop)

This device consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flipflops.

# 6.4.14374xx640 (Octal Bus Transceiver)

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

**FUNCTION TABLE**

| CONTROL INPUTS | | OPERATION | |
|---|---|---|---|
| $\overline{G}$ | DIR | LS640 LS642 | LS641 LS645 |
| L | L | $\overline{B}$ data to A bus | B data to A bus |
| L | H | $\overline{A}$ data to B bus | A data to B bus |
| H | X | Isolation | Isolation |

# 6.4.14474xx645 (Octal Bus Transceiver)

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

**FUNCTION TABLE**

| CONTROL INPUTS | | OPERATION | |
|---|---|---|---|
| $\overline{G}$ | DIR | LS640 LS642 | LS641 LS645 |
| L | L | $\overline{B}$ data to A bus | B data to A bus |
| L | H | $\overline{A}$ data to B bus | A data to B bus |
| H | X | Isolation | Isolation |

# 6.4.14574xx69 (Dual 4-bit Binary Counter)

Counter number one has two sections - counter A (divide-by-2 section) and counter B, C, D (divide-by-8 section). Counter number two has only divide-by-sixteen section.

4-Bit counter truth table:

| $\overline{1CLR}$ | $\overline{2CLR}$ | 1QA | 1QB | 1QC | 1QD | 2QA | 2QB | 2QC | 2QD |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | COUNT | | | | COUNT | | | |
| 1 | 0 | COUNT | | | | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | COUNT | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# 6.4.14674xx72 (AND-gated JK MS-SLV FF (pre, clr))

This device is equipped with an active-low pre and active-low clr. Therefore, the flip-flop begins accepting input from the JK input when the preset and clear are both high (hence AND-gated).

AND-gated JK flip-flop truth table:

| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
|---|---|---|---|---|---|---|
| 0 | 1 | X | X | X | 1 | 0 |
| 1 | 0 | X | X | X | 0 | 1 |
| 0 | 0 | X | X | X | UNSTABLE | |
| 1 | 1 | · | 0 | 0 | Q0 | $\overline{Q0}$ |
| 1 | 1 | · | 1 | 0 | 1 | 0 |
| 1 | 1 | · | 0 | 1 | 0 | 1 |
| 1 | 1 | · | 1 | 1 | Toggle | |

· = triggers on pulse (level sensitive)

# 6.4.14774xx73 (Dual JK FF (clr))

This device contains 2-independent JK flip-flops.

JK flip-flop truth table:

| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
|---|---|---|---|---|---|
| 0 | X | X | X | 0 | 1 |
| 1 | · | 0 | 0 | Hold | |
| 1 | · | 1 | 0 | 1 | 0 |
| 1 | · | 0 | 1 | 0 | 1 |
| 1 | · | 1 | 1 | Toggle | |

· = triggers on pulse (level sensitive)

# 6.4.14874xx74 (Dual D-type FF (pre, clr))

This device is equipped with active-low preset and active-low clear inputs.

D-type positive-edge-triggered flip-flop truth table:

| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
|---|---|---|---|---|---|
| 0 | 1 | X | X | 1 | 0 |
| 1 | 0 | X | X | 0 | 1 |
| 0 | 0 | X | X | 1 | 1 |
| 1 | 1 | · | 1 | 1 | 0 |
| 1 | 1 | · | 0 | 0 | 1 |
| 1 | 1 | 0 | X | Hold | |

· = positive edge-triggered

# 6.4.14974xx75 (4-bit Bistable Latches)

This device features complementary Q and $\overline{Q}$ outputs from a 4-bit latch.

Bistable latch truth table:

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| **D** | **C** | **Q** | **$\overline{Q}$** |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| X | 0 | Q0 | $\overline{Q0}$ |

# 6.4.15074xx76 (Dual JK FF (pre, clr))

This device contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs.

JK flip-flop truth table:

| **$\overline{PRE}$** | **$\overline{CLR}$** | **CLK** | **J** | **K** | **Q** | **$\overline{Q}$** |
|---|---|---|---|---|---|---|
| 0 | 1 | X | X | X | 1 | 0 |
| 1 | 0 | X | X | X | 0 | 1 |
| 0 | 0 | X | X | X | 1 | 1 |
| 1 | 1 | · | 0 | 0 | Hold | |
| 1 | 1 | · | 1 | 0 | 1 | 0 |
| 1 | 1 | · | 0 | 1 | 0 | 1 |
| 1 | 1 | · | 1 | 1 | Toggle | |

· = pulse triggered (level sensitive)

# 6.4.15174xx77 (4-bit Bistable Latches)

This 4-bit latch is available in a 14-pin flat package.

Sample bistable latch truth table:

| **D** | **C** | **L** | **H** |
|---|---|---|---|
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |
| X | 0 | Hold | |

# 6.4.15274xx78 (Dual JK FF (pre, com clk & clr))

The 7478 contains two negative-edge triggered flip-flops with individual JK, individual preset, common clock and common clear inputs.

JK flip-flop truth table:

| PRESET | CLEAR | J | K | CLOCK | Q | $\overline{Q}$ | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | X | X | X | 1 | 0 | |
| 1 | 0 | X | X | X | 0 | 1 | |
| 0 | 0 | X | X | X | 1* | 1* | (unstable) |
| 1 | 1 | 0 | 0 | Ø | (no change) | | |
| 1 | 1 | 0 | 1 | Ø | 0 | 1 | |
| 1 | 1 | 1 | 0 | Ø | 1 | 0 | |
| 1 | 1 | 1 | 1 | Ø | (toggle) | | |
| 1 | 1 | X | X | 1 | (no change) | | |

* = This configuration will not persist when preset and clear are inactive.

Ø = Transition from high to low.

# 6.4.15374xx82 (2-bit Bin Full Adder)

This device performs the addition of two 2-bit binary numbers.

2-bit binary full adder truth table:

| INPUTS | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | WHEN CO = L | | | WHEN CO = H | | |
| A1 | B1 | A2 | B2 | S1 | S2 | C2 | S1 | S2 | C2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

# 6.4.15474xx821 (10-Bit D-type Flip-Flop)

This device consists of ten D-type edge-triggered flipflops. This device has 3-STATE true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW the content of the flip-flops are available at the

outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

| Inputs | | | Internal | Output | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | CP | D | $\overline{Q}$ | O | |
| H | H | X | NC | Z | Hold |
| H | L | X | NC | Z | Hold |
| H | ⌐ | L | H | Z | Load |
| H | ⌐ | H | L | Z | Load |
| L | ⌐ | L | H | L | Data Available |
| L | ⌐ | H | L | H | Data Available |
| L | H | X | NC | NC | No Change in Data |
| L | L | X | NC | NC | No Change in Data |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

# 6.4.15574xx823 (9-Bit D-type Flip-Flop)

This device consists of nine D-type edge-triggered flip-flops. It has 3-STATE true outputs and is organized in broadside pinning. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the OE LOW the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 74F823 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. When the $\overline{CLR}$ is LOW and the OE is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is

HIGH, the outputs do not change state regardless of the data or clock inputs transitions. This device is ideal for parity bus interfacing in high performance systems.

| Inputs | | | | | Internal | Output | Function |
|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{EN}$ | CP | D | $\overline{Q}$ | O | |
| H | H | L | H | X | NC | Z | Hold |
| H | H | L | L | X | NC | Z | Hold |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | Hold |
| H | L | X | X | X | H | Z | Clear |
| L | L | X | X | X | H | L | Clear |
| H | H | L | ⌐ | H | H | Z | Load |
| H | H | L | ⌐ | H | L | Z | Load |
| L | H | L | ⌐ | L | H | L | Data Available |
| L | H | L | ⌐ | H | L | H | Data Available |
| L | H | L | H | X | NC | NC | No Change in Data |
| L | H | L | L | X | NC | NC | No Change in Data |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

# 6.4.15674xx825 (8-Bit D-Type Flip-Flop)

This device consists of eight D-type edge-triggered flip-flops. This device has 3-STATE true outputs and is organized in broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops. The 74F825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. When the $\overline{CLR}$ is LOW and the OE is LOW the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition.

When the $\overline{EN}$ is HIGH the outputs do not change state, regardless of the data or clock input transitions.

| Inputs | | | | | Internal | Output | Function |
|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{EN}$ | CP | D | $\overline{Q}$ | O | |
| H | H | L | H | X | NC | Z | Hold |
| H | H | L | L | X | NC | Z | Hold |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | Hold |
| H | L | X | X | X | H | Z | Clear |
| L | L | X | X | X | H | L | Clear |
| H | H | L | ⌐ | L | H | Z | Load |
| H | H | L | ⌐ | H | L | Z | Load |
| L | H | L | ⌐ | L | H | L | Data Available |
| L | H | L | ⌐ | H | L | H | Data Available |
| L | H | L | H | X | NC | NC | No Change in Data |
| L | H | L | L | X | NC | NC | No Change in Data |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

# 6.4.15774xx827 (10-Bit Buffers/Line Drivers)

This device is a line driver designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have 3-STATE outputs controlled by the Output Enable ($\overline{OE}$) pins. The outputs can sink 64 mA and source 15 mA. Input clamp diodes limit high-speed termination effects.

# 6.4.15874xx828 (10-Bit Buffers/Line Drivers)

This device is a line driver designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have 3-STATE outputs controlled by the Output Enable ($\overline{OE}$) pins. The outputs can sink 64 mA and source 15 mA. Input clamp diodes limit high-speed termination effects.

# 6.4.15974xx83 (4-bit Bin Full Adder)

This device performs the addition of two 4-bit binary numbers. It features full internal look-ahead across all four bits generating the carry term in ten nanoseconds typically.

# 6.4.16074xx85 (4-bit Mag COMP)

This 4-bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes.

4-bit magnitude comparator truth table:

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| **A3, B3** | **A2, B2** | **A1, B1** | **A0, B0** | **A>B** | **A<B** | **A=B** | **A>B** | **A<B** | **A=B** |
| A3>B3 | X | X | X | X | X | X | 1 | 0 | 0 |
| A3<B3 | X | X | X | X | X | X | 0 | 1 | 0 |
| A3=B3 | A2>B2 | X | X | X | X | X | 1 | 0 | 0 |
| A3=B3 | A2<B2 | X | X | X | X | X | 0 | 1 | 0 |
| A3=B3 | A2=B2 | A1>B1 | X | X | X | X | 1 | 0 | 0 |
| A3=B3 | A2=B2 | A1<B1 | X | X | X | X | 0 | 1 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0>B0 | X | X | X | 1 | 0 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0<B0 | X | X | X | 0 | 1 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 1 | 0 | 0 | 1 | 0 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 0 | 1 | 0 | 0 | 1 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 0 | 0 | 1 | 0 | 0 | 1 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | X | X | 1 | 0 | 0 | 1 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 1 | 1 | 0 | 0 | 0 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 0 | 0 | 0 | 1 | 1 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 0 | 1 | 1 | 0 | 1 | 1 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 1 | 0 | 1 | 1 | 0 | 1 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 1 | 1 | 1 | 1 | 1 | 1 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 1 | 1 | 0 | 1 | 1 | 0 |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | 0 | 0 | 0 | 0 | 0 | 0 |

# 6.4.16174xx86 (Quad 2-In XOR)

Logic function:

$Y = \overline{A} \oplus \overline{B}$

EXCLUSIVE-OR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# 6.4.16274xx90 (Decade Counter)

The 7490 counts from 0 to 9 in binary. It contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

Decade counter truth table:

| RESET INPUTS | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| R0(1) | R0(2) | R9(1) | R9(2) | Qd | Qc | Qb | Qa |
| 1 | 1 | 0 | X | 0 | 0 | 0 | 0 |
| 1 | 1 | X | 0 | 0 | 0 | 0 | 0 |
| X | X | 1 | 1 | 1 | 0 | 0 | 1 |
| X | 0 | X | 0 | COUNT | | | |
| 0 | X | 0 | X | COUNT | | | |
| 0 | X | X | 0 | COUNT | | | |
| X | 0 | 0 | X | COUNT | | | |

# 6.4.16374xx91 (8-bit Shift Reg)

This 8-bit shift register contains eight R-S master-slave flip-flops, input gating, and a clock driver.

Shift register truth table:

| A | B | Qh | $\overline{Q}$h |
|---|---|---|---|
| 1 | 1 | 1 | 0 |
| 0 | X | 0 | 1 |
| X | 0 | 0 | 1 |

# 6.4.16474xx92 (Divide-by-twelve Counter)

The 7492 counts from 0 to 11 in binary. It contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-six.

Counter truth table:

| RESET INPUTS | | OUTPUT | | | |
|---|---|---|---|---|---|
| **RO1** | **RO2** | **Qd** | **Qc** | **Qb** | **Qa** |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | X | Count | | | |
| X | 0 | Count | | | |

# 6.4.16574xx93 (4-bit Binary Counter)

The 7493 counts from 0 to 15 in binary. It contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

Binary counter truth table:

| RESET INPUTS | | OUTPUT | | | |
|---|---|---|---|---|---|
| **RO1** | **RO2** | **Qd** | **Qc** | **Qb** | **Qa** |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | X | Count | | | |
| X | 0 | Count | | | |

# Chapter 7
# CMOS

## 7.1 CMOS Overview

The complementary MOS (CMOS) logic family uses both P- and N-channel MOSFETS in the same circuit. CMOS is faster and consumes less power than the other MOS families.

CMOS ICs provide not only all of the same logic functions available in TTL, but also several special functions not provided by TTL.

The 74C series is pin-compatible (pin configuration of the two ICs are the same) with and functionally equivalent to TTL devices with the same number. Many but not all functions that are available in TTL are also available in the 74C series. It is possible then to replace some TTL circuits with an equivalent design.

The 74HC/HCT series is an improved version of the 74C series. It has a tenfold increase in switching speed compared to the 74LS devies and a higher output current capability than that of the 74C. The 74HC/HCT ICs are pin-compatible with and functionally equivalent to TTL ICs with the same number. 74HCT devices are electrically compatible with TTL, but devices from the 74C series are not.

### 7.1.1 Power-Supply Voltage

The 4000/14000 series and 74C series devices can operate with $V_{DD}$ values ranging from 3 to 15 V. The 74HC/HCT and 74AC/ACT series operate over a range of supply voltages between 2 and 6 V.

### 7.1.2 Logic Voltage Levels

The input and ouput voltage levels are different for each CMOS series. The $V_{OL}$ for the CMOS devices is close to 0 V and the $V_{ON}$ is close to 5 V. The required input voltage levels

are greater for CMOS than for TTL, except for the 74 ACT series. These series are designed to be electrically comparable with TTL, so they must accept the same input voltage levels as TTL.

### 7.1.3 Noise Margins

The CMOS devices have greater noise margins than TTL.

### 7.1.4 Power Dissipation

The power dissipation of a CMOS logic circuit is very low when the circuit is in a static state.

The pwoer dissipation of a CMOS IC increases in proportion to the frequency at which the circuits are switching states.

## 7.2 4000 Series ICs

### 7.2.1 4000 (Dual 3-In NOR and INVERTER)

This device contains dual 3-input NOR and Inverters gates.

Logic function:

$$O_1 = \overline{I_1+I_2+I_3}$$

NOR gate truth table:

| I1 | I2 | I3 | O1 |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |

## 7.2.2 4001 (Quad 2-In NOR)

This device contains four independent 2-input NOR gates.

Logic function:

$$O_1 = \overline{I_1+I_2}$$

NOR gate truth table:

| I1 | I2 | O1 |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

## 7.2.3 4002 (Dual 4-In NOR)

This device contains two independent 4-input NOR gates.

Logic function:

$$O_1 = \overline{I_1+I_2+I_3+I_4}$$

NOR gate truth table:

| I1 | I2 | I3 | I4 | O1 |
|---|---|---|---|---|
| 1 | X | X | X | 0 |
| X | 1 | X | X | 0 |
| X | X | 1 | X | 0 |
| X | X | X | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 |

## 7.2.4 4007 (Dual Com Pair/Inv)

This device is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors.

## 7.2.5 4008 (4-bit Binary Full Adder)

This device is capable of adding two 4-bit binary numbers together.

Logic function:

$S = CIN \oplus A \oplus B$
$C = AB+BCOUT+ACOUT$

4-bit binary adder truth table:

| INPUTS | | | | | | | | | OUTPUTS |
|---|---|---|---|---|---|---|---|---|---|
| **CIN** | **A1** | **B1** | **A2** | **B2** | **A3** | **B3** | **A4** | **B4** | **COUT** |
| X | 1 | X | X | 1 | X | 1 | X | 1 | 1 |
| X | X | X | 1 | X | X | 1 | X | 1 | 1 |
| X | X | X | X | X | 1 | X | X | 1 | 1 |
| X | X | X | X | X | X | X | 1 | X | 1 |
| 1 | X | 1 | X | 1 | X | 1 | X | 1 | 1 |
| X | X | X | X | X | X | X | X | X | 0 |

## 7.2.6 4010 (Hex BUFFER)

This device contains six independent BUFFER gates.

Logic function:

$Y = \overline{A}$

BUFFER gate truth table:

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

## 7.2.7 40106 (Hex INVERTER (Schmitt))

This device contains six independent INVERTER gates. Due the to the Schmitt-trigger action, this device is ideal for circuits that are susceptible to unwanted small signals, such as noise.

Logic function:

$$Y = \overline{A}$$

INVERTER gate truth table:

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

## 7.2.8 4011 (Quad 2-In NAND)

This device contains four independent 2-input NAND gates.

Logic function:

$$O_1 = \overline{I_1 I_2}$$

NAND gate truth table:

| I1 | I2 | O1 |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 7.2.9 4012 (Dual 4-In NAND)

This device contains two independent 4-input NAND gates.

Logic function:

$$O_1 = \overline{I_1 + I_2 + I_3 + I_4}$$

NAND gate truth table:

| INPUTS | | | | OUTPUTS |
|---|---|---|---|---|
| I1 | I2 | I3 | I4 | O1 |
| 1 | 1 | 1 | 1 | 0 |
| 0 | X | X | X | 1 |
| X | 0 | X | X | 1 |
| X | X | 0 | X | 1 |
| X | X | X | 0 | 1 |

## 7.2.10 4013 (Dual D-type FF (+edge))

The 4013 device is a dual D-type flip-flop that features independent set direct ($S_D$), clear direct ($C_D$), clock inputs (CP) and outputs (O,$\overline{O}$).

D-type positive edge-triggered flip-flop truth table:

| $\overline{SD}$ | $\overline{CD}$ | CP | D | O | $\overline{O}$ |
|---|---|---|---|---|---|
| 1 | 0 | X | X | 1 | 0 |
| 0 | 1 | X | X | 0 | 1 |
| 1 | 1 | X | X | 1 | 1 |
| 0 | 0 | · | 0 | 0 | 1 |
| 0 | 0 | · | 1 | 1 | 0 |

· = positive edge-triggered

## 7.2.11 4014 (8-bit Static Shift Reg)

The 4014 device is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs ($P_0$ to $P_7$), a synchronous serial data input ($D_S$), a synchronous parallel enable input (PE), a LOW to HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages ($O_5$ to $O_7$).

Following are two 8-bit static shift register truth tables.

Serial Operation:

| | INPUTS | | | | | | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **n** | **PE** | **DS** | **>CLK** | **P0** | **P1** | **P2** | **P3** | **P4** | **P5** | **P6** | **P7** | **O5** | **O6** | **O7** |
| 1 | 0 | D1 | · | X | X | X | X | X | X | X | X | X | X | X |
| 2 | 0 | D2 | · | X | X | X | X | X | X | X | X | X | X | X |
| 3 | 0 | D3 | · | X | X | X | X | X | X | X | X | X | X | X |
| 4 | 0 | D4 | · | X | X | X | X | X | X | X | X | X | X | X |
| 5 | 0 | D5 | · | X | X | X | X | X | X | X | X | X | X | X |
| 6 | 0 | D6 | · | X | X | X | X | X | X | X | X | D1 | X | X |
| 7 | 0 | D7 | · | X | X | X | X | X | X | X | X | D2 | D1 | X |
| 9 | 0 | D8 | · | X | X | X | X | X | X | X | X | D3 | D2 | D1 |
| 10 | 0 | D9 | · | X | X | X | X | X | X | X | X | D4 | D3 | D2 |
| X | X | X | , | X | X | X | X | X | X | X | X | no change | | |

Parallel Operation:

| | | INPUTS | | | | | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PE** | **DS** | **>CLK** | **P0** | **P1** | **P2** | **P3** | **P4** | **P5** | **P6** | **P7** | **O5** | **O6** | **O7** |
| 1 | X | · | X | X | X | X | X | X | X | X | P5 | P6 | P7 |
| 1 | X | , | X | X | X | X | X | X | X | X | no change | | |

# 7.2.12 4015 (Dual 4-bit Static Shift Reg)

The 4015 device is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs ($O_0$ to $O_3$) and an overriding asynchronous master reset input (MR).

Shift register truth table:

| n | CP | D | MR | O0 | O1 | O2 | O3 |
|---|---|---|---|---|---|---|---|
| 1 | · | D1 | 0 | D1 | X | X | X |
| 2 | · | D2 | 0 | D2 | D1 | X | X |
| 3 | · | D3 | 0 | D3 | D2 | D1 | X |
| 4 | · | D4 | 0 | D4 | D3 | D2 | D1 |
| | , | X | 0 | | no change | | |
| | X | X | 1 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| 1 | = | HIGH state (the more positive voltage) |
| 0 | = | LOW state (the less positive voltage) |
| X | = | state is immaterial |
| · | = | positive-going transition |
| , | = | negative-going transition |
| Dn | = | either HIGH or LOW |
| n | = | number of clock pulse transitions |

# 7.2.13 40160 (4-bit Dec Counter)

The 40160 device is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), an overriding asynchronous master reset ($\overline{MR}$), four parallel data inputs (P0 to P3), three synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O0 to O3) and a terminal count output (TC).

## 7.2.14 40161 (4-bit Bin Counter)

The 40161 device is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), an overriding asynchronous master reset ($\overline{MR}$), four parallel data inputs (P0 to P3), three synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O0 to O3) and a terminal count output (TC).

## 7.2.15 40162 (4-bit Dec Counter)

The 40162 device is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), four synchronous parallel data inputs (P0 to P3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP) and count enable trickle (CET)), and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O0 to O3) and a terminal count output (TC).

## 7.2.16 40163 (4-bit Bin Counter)

The 40163 device is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), four synchronous parallel data inputs (P0 to P3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP) and count enable trickle (CET)), and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O0 to O3) and a terminal count output (TC).

## 7.2.17 4017 (5-stage Johnson Counter)

The 4017 device is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs ($O_0$ to $O_9$), an active LOW output from the most significant flip-flop ($\overline{O}_{5\text{-}9}$), active HIGH and active LOW clock inputs ($CP_0$, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

5-stage Johnson counter truth table:

| MR | CP0 | CP1 | OPERATION |
|---|---|---|---|
| 1 | X | X | O0 = O5-9 = H; O1 to O9 = L |
| 0 | 1 | , | Counter advances |
| 0 | · | 0 | Counter advances |
| 0 | 0 | X | No change |
| 0 | X | 1 | No change |
| 0 | 1 | · | No change |
| 0 | , | 0 | No change |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial
· = positive-going transition
, = negative-going transition
n = number of clock pulse transitions

## 7.2.18 40174 (Hex D-type Flip-flop)

The 40174 device is a hex edge-triggered D-type flip-flop with six data inputs (D0 to D5), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), and six buffered outputs (Q0 to Q5).

# 7.2.19 40175 (Quad D-type Flip-flop)

This device is a quadruple edge-triggered D-type flip-flop with four data inputs ($D_0$ to $D_3$), a clock input (CP), an overriding asynchronous master rest input ($\overline{MR}$), four buffered outputs ($Q_0$ to $Q_3$), and four complementary buffered outputs ($\overline{Q}_0$ to $\overline{Q}_3$).

Quadruple D-type flip-flop truth table:

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| **CP** | **D** | **$\overline{MR}$** | **Q** | **$\overline{Q}$** |
| | 1 | 1 | 1 | 0 |
| | 0 | 1 | 0 | 1 |
| | X | 1 | no change | no change |
| X | X | 0 | 0 | 1 |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial
= positive-going transition
= negative-going transition

## 7.2.20 4018 (5-stage Johnson Counter)

The 4018 device is a 5-stage Johnson counter with a clock input (CP), a data input (D), an asynchronous parallel load input (PL), five parallel inputs (P0 to P4), five active LOW buffered outputs ($\overline{O}0$ to $\overline{O}4$), and an overriding asynchronous master reset input ($\overline{MR}$).

5-stage Johnson counter truth table:

| Counter mode; divide by | Connect D input to | Remarks |
|---|---|---|
| 10 | $\overline{O4}$ | no external components needed |
| 8 | $\overline{O3}$ | |
| 6 | $\overline{O2}$ | |
| 4 | $\overline{O1}$ | |
| 2 | $\overline{O0}$ | |
| 9 | $\overline{O3} \bullet \overline{O4}$ | AND gate needed; counter skips all HIGH states |
| 7 | $\overline{O2} \bullet \overline{O3}$ | |
| 5 | $\overline{O1} \bullet \overline{O2}$ | |
| 3 | $\overline{O0} \bullet \overline{O1}$ | |

## 7.2.21 4019 (Quad 2-In MUX)

The 4019 device provides four multiplexing circuits with common select inputs ($S_A$, $S_B$); each circuit contains two inputs ($A_n$, $B_n$) and one output ($O_n$).

Multiplexer truth table:

| SELECT | | INPUTS | | OUTPUTS |
|---|---|---|---|---|
| Sa | Sb | A0 | B0 | O0 |
| 0 | 0 | X | X | 0 |
| 1 | 0 | 0 | X | 0 |
| 1 | 0 | 1 | X | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 1 | X | 1 | 1 |
| 1 | 1 | 1 | X | 1 |
| 1 | 1 | X | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |

## 7.2.22 40192 (4-bit Dec Counter)

The 40192 device is a 4-bit synchronous up/down decade counter with a count-up clock input (CPU), a count-down clock input (CPD), an asynchronous parallel load input ($\overline{PL}$), four parallel data inputs (P0 to P3), an asynchronous master reset input (MR), four counter outputs (O0 to O3), an active LOW terminal count-up (carry) output ($\overline{TC}$U) and an active LOW terminal count-down (borrow) output ($\overline{TC}$D).

## 7.2.23 40193 (4-bit Bin Counter)

The 40193 device is a 4-bit synchronous up/down binary counter with a count-up clock input (CPU), a count-down clock input (CPD), an asynchronous parallel load input ($\overline{PL}$), four parallel data inputs (P0 to P3), an asynchronous master reset input (MR), four counter outputs (O0 to O3), an active LOW terminal count-up (carry) output ($\overline{TC}$U) and an active LOW terminal count-down (borrow) output ($\overline{TC}$D).

## 7.2.24 40194 (4-bit Shift Register)

The 40194 device is a 4-bit bidirectional shift register with two mode control inputs (S0 and S1), a clock input (CP), a serial data shift left input (DSL), a serial data shift right input (DSR), four parallel data inputs (P0 to P3), an overriding asynchronous master reset input ($\overline{MR}$), and four buffered parallel outputs (O0 to O3).

## 7.2.25 40195 (4-bit Shift Register)

The 40195 device is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P0 to P3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input ($\overline{PE}$), buffered parallel outputs from all 4-bit positions (O0 to O3), a buffered inverted output from the last bit position ($\overline{O}3$) and an overriding asynchronous master reset input ($\overline{MR}$).

## 7.2.26 4020 (14-stage Bin Counter)

The 4020 device is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs.

## 7.2.27 4021 (8-bit Static Shift Register)

The 4021 device is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input ($D_S$), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs, and buffered parallel outputs from the last three stages.

## 7.2.28 4023 (Tri 3-In NAND)

This device contains three independent 3-input NAND gates.

Logic function:

$$O = \overline{I_1+I_2+I_3}$$

NAND gate truth table:

| $I_1$ | $I_2$ | $I_3$ | $O_1$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 |

## 7.2.29 4024 (7-stage Binary Counter)

The 4024 is a 7-stage binary ripple counter. A high on MR (Master Reset) forces all counter stages and outputs low. The 4024 counts from 0 to 15 in binary on every negative (high to low) transition of the clock pulse.

## 7.2.30 40240 (Dual Octal Inv Buffer)

The 40240 device is a dual octal inverting buffer with 3-state outputs.

| INPUTS | | OUTPUT |
|---|---|---|
| $I_n$ | $\overline{EO}$ | $O_n$ |
| H | L | L |
| L | L | H |
| X | H | Z |

## 7.2.31 40244 (Dual Octal Non-inv Buffer)

The 40244 device is a dual octal non-inverting buffer with 3-state outputs.

| INPUTS | | OUTPUT |
|---|---|---|
| $I_n$ | $\overline{EO}$ | $O_n$ |
| H | L | H |
| L | L | L |
| X | H | Z |

## 7.2.32 40245 (Octal Bus Transceiver)

The 40245 device, an octal bus transceiver with 3-state outputs, is designed for 8-line asynchronous, 2-way data communication between data buses.

| INPUTS | | INPUTS/OUTPUTS | |
|---|---|---|---|
| $\overline{EO}$ | DR | $A_n$ | $B_n$ |
| L | L | A = B | input |
| L | H | input | B = A |
| H | X | Z | Z |

## 7.2.33 4025 (Tri 3-In NOR)

This device contains three independent 3-input NOR gates.

Logic function:

$$O = \overline{I_1+I_2+I_3}$$

NOR gate truth table:

| $I_1$ | $I_2$ | $I_3$ | $O_1$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |

## 7.2.34 4027 (Dual JK FF (+edge, pre, clr))

This device contains two independent JK flip-flops with separate preset and clear inputs.

Sample JK flip-flop truth table:

| SD | CD | CP | J | K | On | $\overline{On}$ |
|---|---|---|---|---|---|---|
| 1 | 0 | X | X | X | 1 | 0 |
| 0 | 1 | X | X | X | 0 | 1 |
| 1 | 1 | X | X | X | 1 | 1 |
| 0 | 0 | · | 0 | 0 | Hold | |
| 0 | 0 | · | 1 | 0 | 1 | 0 |
| 0 | 0 | · | 0 | 1 | 0 | 1 |
| 0 | 0 | · | 1 | 1 | Toggle | |

· = triggers on POSITIVE pulse

## 7.2.35 4028 (1-of-10 Dec)

The 4028 device is a 4-bit BCD to 1-of-10 active HIGH decoder.

1-of-10 decoder truth table:

| BCD INPUTS | | | | DECIMAL OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | O0 | O1 | O2 | O3 | O4 | O5 | O6 | O7 | O8 | O9 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| *Extraordinary states | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# 7.2.36 4029 (4-bit Bin/BCD Dec Counter)

The 4029 is a synchronous edge-triggered up/down 4-bit binary/BCD decade counter with a clock input (CP), an active LOW count enable input ($\overline{CE}$), an up/down control input (UP/$\overline{DN}$), a binary/decade control input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P0 to P3), four parallel buffered outputs (O0 to O3) and an active LOW terminal count output ($\overline{TC}$).

4-bit binary/BCD decade counter truth table:

| PL | BIN/$\overline{DEC}$ | UP/$\overline{DN}$ | $\overline{CE}$ | CP | mode |
|---|---|---|---|---|---|
| 1 | X | X | X | X | parallel load (Pn → On) |
| 0 | X | X | 1 | X | no change |
| 0 | 0 | 0 | 0 | | count-down, decade |
| 0 | 0 | 1 | 0 | | count-up, decade |
| 0 | 1 | 0 | 0 | | count-down, binary |
| 0 | 1 | 1 | 0 | | count-up, binary |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial
= positive-going clock pulse edge

# 7.2.37 4030 (Quad 2-In XOR)

This device contains four independent 2-input EXCLUSIVE-OR gates.

Logic function:

$O = I_1 \oplus I_2$

EXCLUSIVE-OR gate truth table:

| I1 | I2 | O1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# 7.2.38 4032 (Triple Serial Adder)

The 4032 triple serial adder has the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for this device.

# 7.2.39 4035 (4-bit Shift Register)

The 4035 device is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P0 to P3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O0 to O3), a true/complement input (T/$\overline{C}$) and an overriding asynchronous master reset input (MR).

Following are two shift register truth tables.

Serial operation first stage:

| | INPUTS | | | OUTPUT | |
|---|---|---|---|---|---|
| CP | J | $\overline{K}$ | MR | $O_0$+1 | MODE OF OPERATION |
| | 1 | 1 | 0 | 1 | D flip-flop |
| | 0 | 0 | 0 | 0 | D flip-flop |
| | 1 | 0 | 0 | $\overline{O}_0$ | toggle |
| | 0 | 1 | 0 | $O_0$ | no change |
| X | X | X | 1 | 0 | reset |

Parallel operation:

| CP | INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|
| | P0 | P1 | P2 | P3 | O0 | O1 | O2 | O3 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

= positive-going transition
1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial

## 7.2.40 40373 (Octal Trans Latch)

The 40373 device is an 8-bit transparent latch with 3-state buffered outputs.

| OPERATING MODES | INPUTS | | | INTERNAL REGISTER | OUTPUTS $O_0$ TO $O_7$ |
|---|---|---|---|---|---|
| | $\overline{EO}$ | E | $D_n$ | | |
| enable & read register | L | H | L | L | L |
| | L | H | H | H | H |
| latch & read register | L | L | l | L | L |
| | L | L | h | H | H |
| latch register & disable outputs | H | L | l | L | Z |
| | H | L | h | H | Z |

## 7.2.41 40374 (Octal D-type Flip-flop)

The 40374 device is an octal D-type flip-flop with 3-state buffered outputs with a common clock input (CP). It used primarily as an 8-bit positive edge-triggered storage register for interfacing with a 3-state bus.

| OPERATING MODES | INPUTS | | | INTERNAL REGISTER | OUTPUTS $O_0$ TO $O_7$ |
|---|---|---|---|---|---|
| | $\overline{EO}$ | CP | $D_n$ | | |
| load & read register | L | ⌐ | l | L | L |
| | L | ⌐ | h | H | H |
| load register & disable outputs | H | ⌐ | l | L | Z |
| | H | ⌐ | h | H | Z |

## 7.2.42 4038 (Triple Serial Adder)

The 4038 triple serial adder has the clock and carry reset inputs common to all three adders. The carry is added on the negative-going clock transition for this device.

## 7.2.43 4040 (12-stage Binary Counter)

The 4040 device is a 12-stage binary ripple counter with a clock input (CP), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs ($O_0$ to $O_{11}$).

12-stage binary counter truth table:

| $\overline{CP}$ | MR | O0-O11 |
|---|---|---|
| , | 0 | Count |
| , | 1 | 0 |

## 7.2.44 4041 (Quad True/Complement BUFFER)

This device provides both inverted and non-inverted buffered outputs for each input.

Logic function:

$\overline{O} = \overline{I}$

$O = I$

Buffer gate truth table:

| I | 0 | $\overline{O}$ |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 0 |

## 7.2.45 4042 (Quad D-latch)

This device contains four independent D-latches.

D-latch truth table:

| $E_0$ | $E_1$ | OUTPUT $O_n$ |
|---|---|---|
| L | L | $D_n$ |
| L | H | latched |
| H | L | latched |
| H | H | $D_n$ |

## 7.2.46 4043 (Quad RS latch w/3-state Out)

This device contains four independent RS-latches with 3-state outputs.

RS-latch truth table:

| EO | Sn | Rn | On |
|---|---|---|---|
| 0 | X | X | Z |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 1 |
| 1 | 0 | 0 | Latched |

## 7.2.47 4044 (Quad RS latch w/3-state Out)

This device contains four independent RS-latches with 3-state outputs.

RS-latch truth table:

| EO | $\overline{Sn}$ | $\overline{Rn}$ | On |
|---|---|---|---|
| 0 | X | X | Z |
| 1 | 0 | 1 | 1 |
| 1 | X | 0 | 0 |
| 1 | 1 | 1 | Latched |

## 7.2.48 4049 (Hex INVERTER)

This device contains six independent INVERTER gates.

Logic function:

$O = \overline{I}$

INVERTER gate truth table:

| I1 | O1 |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 7.2.49 4050 (Hex BUFFER)

This device contains six independent BUFFER/non-inverting gates.

Logic function:

$Y = \overline{A}$

BUFFER gate truth table:

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

## 7.2.50 4060 (14-Stage Binary Counter & Osc)

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals, ten buffered outputs and an overriding asynchronous master reset input. The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter ($O_3$ to $O_9$ and $O_{11}$ to $O_{13}$ = LOW), independent of other input conditions. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## 7.2.51 4066 (Quad Analog Switches)

The 4066 device has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E).

When the C input is high, the input/outputs A and B, will pass either digital or analog signals in either direction.

Analog switch truth table:

| C | A B |
|---|---|
| 0 | Z |
| 1 | <-> |

## 7.2.52 4068 (8-In NAND)

Logic function:

$$O_1 = \overline{I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7}$$

NAND gate truth table:

| INPUTS I0 THROUGH I7 | O1 |
|---|---|
| All inputs 1 | 0 |
| One or more inputs | \| |

## 7.2.53 4069 (Hex INVERTER)

This device contains six independent INVERTER gates.

Logic function:

$$A = \overline{Y}$$

INVERTER gate truth table:

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

## 7.2.54 4070 (Quad 2-In XOR)

This device contains four independent 2-input EXCLUSIVE-OR gates.

Logic function:

$$Y = \overline{A} \oplus \overline{B}$$

EXCLUSIVE-OR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## 7.2.55 4071 (Quad 2-In OR)

This device contains four independent 2-input OR gates.

Logic function:

$Y = A+B$

OR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

## 7.2.56 4072 (Dual 4-In OR)

The 4072 device provides the positive dual 4-input OR function.

Logic function:

$Y = A+B+C+D$

4-input OR gate truth table:

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## 7.2.57 4073 (Tri 3-In AND)

This device contains three independent 3-input AND gates.

Logic function:

$Y = ABC$

AND gate truth table:

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |

# 7.2.58 4075 (Tri 3-In OR)

This device contains three independent 3-input OR gates.

Logic function:

$Y = A+B+C$

OR gate truth table:

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

# 7.2.59 4076 (Quad D-type Reg w/3-state Out)

The 4076 device is a quadruple edge-triggered D-type flip-flop with four data inputs ($D_0$ to $D_3$), two active LOW data enable inputs ($\overline{ED}_0$ and ($\overline{ED}_1$), a common clock input (CP), four 3-state outputs ($O_0$ to $O_3$), two active LOW output enable inputs ($\overline{EO}_0$ and $\overline{EO}_1$), and an overriding asynchronous master reset input (MR).

D-type register truth table:

| INPUTS | | | | | OUTPUTS |
|---|---|---|---|---|---|
| MR | CP | ED0 | ED1 | Dn | On |
| 1 | X | X | X | X | 0 |
| 0 | · | 1 | X | X | NO CHANGE |
| 0 | · | X | 1 | X | NO CHANGE |
| 0 | · | 0 | 0 | 1 | 1 |
| 0 | · | 0 | 0 | 0 | 0 |
| 0 | , | X | X | X | NO CHANGE |

## 7.2.60 4077 (Quad 2-In XNOR)

This device contains four independent 2-input EXCLUSIVE-NOR gates.

Logic function:

$$O = \overline{A} \oplus \overline{B}$$

EXCLUSIVE-NOR gate truth table:

| An | Bn | On |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## 7.2.61 4078 (8-In NOR)

Logic function:

$$O = \overline{I_0+I_1+I_2+I_3+I_4+I_5+I_6+I_7}$$

8-input NOR gate simplified truth table:

If one or more inputs are high, the output is low.

| INPUTS | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|
| I0 | I1 | I2 | I3 | I4 | I5 | I6 | I7 | O1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | X | X | X | X | X | X | X | 0 |
| X | 1 | X | X | X | X | X | X | 0 |
| X | X | 1 | X | X | X | X | X | 0 |
| X | X | X | 1 | X | X | X | X | 0 |
| X | X | X | X | 1 | X | X | X | 0 |
| X | X | X | X | X | 1 | X | X | 0 |
| X | X | X | X | X | X | 1 | X | 0 |
| X | X | X | X | X | X | X | 1 | 0 |

## 7.2.62 4081 (Quad 2-In AND)

This device contains four independent 2-input AND gates.

Logic function:

Y = AB

AND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## 7.2.63 4082 (Dual 4-In AND)

This device contains two independent 4-input AND gates.

All 4-inputs on each 4-input gate must be high to obtain a high at the output.

Logic function:

Y = ABCD

AND gate truth table:

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

## 7.2.64 4085 (Dual 2-Wide 2-In AND-OR-INVERTER)

This device contains a combination of gates (AND, OR and INVERTER).

Logic function:

$$O_A = \overline{A_0 \bullet A_1 + A_2 \bullet A_3 + A_4}$$

$$O_B = \overline{B_0 \bullet B_1 + B_2 \bullet B_3 + B_4}$$

Inverter gate truth table:

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| **A0** | **A1** | **A2** | **A3** | **A4** | **OA** |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | L |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 |

# 7.2.65 4086 (4-Wide 2-In AND-OR-INVERTER)

This device contains a combination of gates (AND, OR and INVERTER).

Logic function:

$$O = \overline{I_0 I_1 + I_2 I_3 + I_4 I_5 + I_6 I_7 + I_8 + I_9}$$

Inverter gate truth table:

| INPUTS | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|
| I0 | I1 | I2 | I3 | I4 | I5 | I6 | I7 | I8 | ~I9 | O |
| X | X | X | X | X | X | X | X | 1 | X | 0 |
| X | X | X | X | X | X | X | X | X | 0 | 0 |
| 1 | 1 | X | X | X | X | X | X | X | X | 0 |
| X | X | 1 | 1 | X | X | X | X | X | X | 0 |
| X | X | X | X | 1 | 1 | X | X | X | X | 0 |
| X | X | X | X | X | X | 1 | 1 | X | X | 0 |
| ANY OTHER COMBINATION OF INPUTS | | | | | | | | | | 1 |

# 7.2.66 4093 (Quad 2-In NAND (Schmitt))

This device contains four independent 2-input NAND gates. Due the to the Schmitt-trigger action, this device is ideal for circuits that are susceptible to unwanted small signals, such as noise.

Logic function:

$$O = \overline{A1B2}$$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# 7.2.67 4094 (8-stage Serial Shift Register)

The 4094 device is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs O0 to O7.

Shift register truth table:

| INPUTS | | | | PARALLEL OUTPUTS | | SERIAL OUTPUTS | |
|---|---|---|---|---|---|---|---|
| CP | EO | STR | D | $O_0$ | $O_n$ | $O_s$ | $\overline{O}_s$ |
| | 0 | X | X | Z | Z | $\overline{O}_6$ | nc |
| | 0 | X | X | Z | Z | nc | $O_7$ |
| | 1 | 0 | X | nc | nc | $\overline{O}_6$ | nc |
| | 1 | 1 | 0 | 0 | $O_{n-1}$ | $\overline{O}_6$ | nc |
| | 1 | 1 | 1 | 1 | $O_{n-1}$ | $\overline{O}_6$ | nc |
| | 1 | 1 | 1 | nc | nc | nc | $O_7$ |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial
= positive-going transition
= negative-going transition
Z = high impedance off state

# 7.2.68 4099 (8-bit Latch)

The 4099 device is an 8-bit addressable latch. The input for this device is a unidirectional write only port.

**TRUTH TABLE**

| Write Disable | Reset | Addressed Latch | Unaddressed Latches |
|---|---|---|---|
| 0 | 0 | Data | $Q_n$* |
| 0 | 1 | Data | Reset † |
| 1 | 0 | $Q_n$* | $Q_n$* |
| 1 | 1 | Reset | Reset |

*$Q_n$ is previous state of latch.
†Reset to zero state.

# 7.2.69 4502 (Strobed hex INVERTER)

This device contains six independent INVERTER gates.

INVERTER gate truth table:

| Dn | $\overline{E}$ | $\overline{EO}$ | On |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| X | 1 | 0 | 0 |
| X | X | 1 | Z |

# 7.2.70 4503 (Tri-state hex BUFFER w/Strobe)

Four of these six non-inverting buffers (I1 through I4) are enabled by a high on EN1 and the last two (I5 and I6) are enabled by a high on EN2.

Buffer gate truth table:

| I | EN | O |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| X | 1 | Z |

Z = High impedance
X = Don't care

## 7.2.71 4508 (Dual 4-bit latch)

This device contains two independent 4-bit latches.

4-bit latch truth table:

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| MR | ST | $\overline{EO}$ | $D_n$ | $O_n$ |
| L | H | L | H | H |
| L | H | L | L | L |
| L | L | L | X | latched |
| H | X | L | X | L |
| X | X | H | X | Z |

## 7.2.72 4510 (BCD up/down Counter)

BCD up/down counter truth table:

| MR | $\overline{PL}$ | UP/DN | CE | CP | MODE |
|---|---|---|---|---|---|
| 0 | 1 | X | X | X | PARALLEL LOAD |
| 0 | 0 | X | 1 | X | NO CHANGE |
| 0 | 0 | 0 | 0 | · | COUNT DOWN |
| 0 | 0 | 1 | 0 | · | COUNT UP |
| 1 | X | X | X | X | RESET |

# 7.2.73 4511(BCD-to-seven segment latch/Dec)

The 4511 BCD (Binary-Coded Decimal)-to-seven-segment latch decoder translates a 4-bit BCD input into hexadecimal, and outputs high on the output pins corresponding to the hexadecimal representation of the BCD input. There are provisions for lamp testing and for blanking the outputs.

| | INPUTS | | | | | | | OUTPUTS | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DISPLAY** | $\overline{\textbf{EL}}$ | $\overline{\textbf{BI}}$ | $\overline{\textbf{LT}}$ | **D** | **C** | **B** | **A** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| 8 | X | X | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | X | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 8 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| * | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | | | * | | | |

* Depends on BCD code applied during 0 to 1 transition of $\overline{\text{EL}}$

$\overline{\text{EL}}$ = active-low latch enable input
$\overline{\text{BI}}$ = active-low ripple-blanking input
$\overline{\text{LT}}$ = active-low lamp-test input

## 7.2.74 4512 (8-In MUX w/3-state Out)

This device is a 8-input multiplexer with 3-state outputs.

Multiplexer truth table:

TRUTH TABLE

| INPUTS | | | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{EO}$ | $\overline{E}$ | $S_2$ | $S_1$ | $S_0$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | O |
| L | H | X | X | X | X | X | X | X | X | X | X | X | L |
| L | L | L | L | L | L | X | X | X | X | X | X | X | L |
| L | L | L | L | L | H | X | X | X | X | X | X | X | H |
| L | L | L | L | H | X | L | X | X | X | X | X | X | L |
| L | L | L | L | H | X | H | X | X | X | X | X | X | H |
| L | L | L | H | L | X | X | L | X | X | X | X | X | L |
| L | L | L | H | L | X | X | H | X | X | X | X | X | H |
| L | L | L | H | H | X | X | X | L | X | X | X | X | L |
| L | L | L | H | H | X | X | X | H | X | X | X | X | H |
| L | L | H | L | L | X | X | X | X | L | X | X | X | L |
| L | L | H | L | L | X | X | X | X | H | X | X | X | H |
| L | L | H | L | H | X | X | X | X | X | L | X | X | L |
| L | L | H | L | H | X | X | X | X | X | H | X | X | H |
| L | L | H | H | L | X | X | X | X | X | X | L | X | L |
| L | L | H | H | L | X | X | X | X | X | X | H | X | H |
| L | L | H | H | H | X | X | X | X | X | X | X | L | L |
| L | L | H | H | H | X | X | X | X | X | X | X | H | H |
| H | X | X | X | X | X | X | X | X | X | X | X | X | Z |

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   Z = high impedance OFF-state

## 7.2.75 4514 (1-of-16 Dec/DEMUX w/Input latches)

This device is a 1-of-16 decoder/demultiplexer with input latches. The input latches allow for the user to hold a previous input with the enable input while the inputs change.

1-of-16 decoder/demultiplexer truth table:

| INPUTS | | | | | OUTPUTS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}$ | A3 | A2 | A1 | A0 | O0 | O1 | O2 | O3 | O4 | O5 | O6 | O7 | O8 | O9 | O10 | O11 | O12 | O13 | O14 | O15 |
| 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

## 7.2.76 4515 (1-of-16 Dec/DEMUX w/Input latches)

This device is a 1-of-16 decoder/demultiplexer with input latches. The input latches allow for the user to hold a previous input with the enable input while the inputs change.

1-of-16 decoder/demultiplexer truth table:

| INPUTS | | | | | OUTPUTS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}$ | A3 | A2 | A1 | A0 | O0 | O1 | O2 | O3 | O4 | O5 | O6 | O7 | O8 | O9 | O10 | O11 | O12 | O13 | O14 | O15 |
| 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

# 7.2.77 4516 (Binary up/down Counter)

This binary up/down counter counts from 0000 to 1111 in binary (0 to 15 in decimal).

Binary up/down counter truth table:

| MR | $\overline{PL}$ | $\overline{UP/DN}$ | CE | CP | MODE |
|---|---|---|---|---|---|
| 0 | 1 | X | X | X | PARALLEL LOAD |
| 0 | 0 | X | 1 | X | NO CHANGE |
| 0 | 0 | 0 | 0 | · | COUNT DOWN |
| 0 | 0 | 1 | 0 | · | COUNT UP |
| 1 | X | X | X | X | RESET |

# 7.2.78 4518 (Dual BCD Counter)

The 4518 device is a dual 4-bit internally synchronous BCD counter.

BCD counter truth table:

| $\overline{CP0}$ | CP1 | MR | MODE |
|---|---|---|---|
| · | 1 | 0 | COUNTER ADVANCES |
| 0 | , | 0 | COUNTER ADVANCES |
| , | X | 0 | NO CHANGE |
| X | · | 0 | NO CHANGE |
| · | 0 | 0 | NO CHANGE |
| 1 | , | 0 | NO CHANGE |
| X | X | 1 | O0 TO O3 = LOW |

# 7.2.79 4519 (Quad Multiplexer)

The 4519 device provides four multiplexing circuits with common select inputs (SA, SB). Each circuit contains two inputs (An, Bn) and one output (On).

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $S_A$ | $S_B$ | $A_n$ | $B_n$ | $O_n$ |
| L | L | X | X | L |
| H | L | $A_n$ | X | $A_n$ |
| L | H | X | $B_n$ | $B_n$ |
| H | H | L | L | H |
| H | H | H | L | L |
| H | H | L | H | L |
| H | H | H | H | H |

**Notes**

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial

# 7.2.80 4520 (Dual Binary Counter)

The 4520 device is a dual 4-bit internally synchronous binary counter.

Binary counter truth table:

| $\overline{CP0}$ | CP1 | MR | MODE |
|---|---|---|---|
| · | 1 | 0 | COUNTER ADVANCES |
| 0 | , | 0 | COUNTER ADVANCES |
| , | X | 0 | NO CHANGE |
| X | · | 0 | NO CHANGE |
| · | 0 | 0 | NO CHANGE |
| 1 | , | 0 | NO CHANGE |
| X | X | 1 | O0 TO O3 = LOW |

# 7.2.81 4522 (4-bit BCD Down Counter)

The 4522 device is a synchronous programmable 4-bit BCD down counter with an active HIGH and an active LOW clock input (CP0, CP1), an asynchronous parallel load input (PL), four parallel inputs (P0 to P3), a cascade feedback input (CF), four buffered parallel outputs (O0 to O3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

| MR | PL | $CP_0$ | $\overline{CP_1}$ | MODE |
|---|---|---|---|---|
| H | X | X | X | reset (asynchronous) |
| L | H | X | X | preset (asynchronous) |
| L | L | ⎍ | H | no change |
| L | L | L | ⎏ | no change |
| L | L | ⎏ | X | no change |
| L | L | X | ⎍ | no change |
| L | L | ⎍ | L | counter advances |
| L | L | H | ⎏ | counter advances |

**Notes**

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ⎍ = positive-going transition
   ⎏ = negative-going transition

## 7.2.82 4526 (4-bit Bin Down Counter)

The 4526 device is a synchronous programmable 4-bit binary down counter with an active HIGH and an active LOW clock input (CP0, $\overline{CP1}$), an asynchronous parallel load input (PL), four parallel inputs (P0 to P3), a cascade feedback input (CF), four buffered parallel outputs (O0 to O3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

| MR | PL | $CP_0$ | $\overline{CP_1}$ | MODE |
|---|---|---|---|---|
| H | X | X | X | reset (asynchronous) |
| L | H | X | X | preset (asynchronous) |
| L | L | ⎍ | H | no change |
| L | L | L | ⎎ | no change |
| L | L | ⎎ | X | no change |
| L | L | X | ⎍ | no change |
| L | L | ⎍ | L | counter advances |
| L | L | H | ⎎ | counter advances |

**Notes**

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ⎍ = positive-going transition
   ⎎ = negative-going transition

## 7.2.83 4531 (13-input Checker/Generator)

The 4531 device is a parity checker/generator with 13 parity inputs (I0 to I12) and a parity output (O).

Truth table:

| INPUTS | | | | | | | | | | | | | OUTPUTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **I0** | **I1** | **I2** | **I3** | **I4** | **I5** | **I6** | **I7** | **I8** | **I9** | **I10** | **I11** | **I12** | **O** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| any odd number of inputs HIGH | | | | | | | | | | | | | 1 |
| any even number of inputs HIGH | | | | | | | | | | | | | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)

# 7.2.84 4532 (8-bit Priority Enc)

This device is an 8-bit priority encoder.

Priority encoder truth table:

| | INPUTS | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **E1** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **GS** | **O2** | **O1** | **O0** | **EO** |
| 0 | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | X | X | X | X | X | X | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | X | X | X | X | X | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | X | X | X | X | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

# 7.2.85 4539 (Dual 4-input Multiplexer)

The 4539 device is a dual 4-input multiplexer with common select logic. Each multiplexer has four multiplexer inputs (I0 to I3), an active LOW enable input ($\overline{E}$) and a multiplexer output (O).

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $S_0$ | $S_1$ | $\overline{E}_n$ | $O_n$ |
| X | X | H | L |
| L | L | L | $I_0$ |
| H | L | L | $I_1$ |
| L | H | L | $I_2$ |
| H | H | L | $I_3$ |

**Notes**

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial

# 7.2.86 4543 (BCD-to-seven segment latch/dec/driver)

The 4543 device is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (DA to DD), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Oa to Og).

7-segment latch/decoder/driver truth table:

| INPUTS | | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **LD** | **BI** | **PH *** | **DD** | **DC** | **DB** | **DA** | **Oa** | **Ob** | **Oc** | **Od** | **Oe** | **Of** | **Og** | **DISPLAY** |
| X | 1 | 0 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 9 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 0 | 0 | 0 | X | X | X | X | | | | ** | | | | |
| as above | | 1 | | as above | | | | | inverse as above | | | | | as above |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial

* For liquid crystal displays, apply a square-wave to PH.
For common cathode LED displays, select PH = LOW.
For common anode LED displays, select PH = HIGH.

** Depends upon the BCD-code previously applied when LD = HIGH

# 7.2.87 4544 (BCD-to-seven segment latch/dec)

The 4544 BCD (Binary-Coded Decimal) -to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts. It is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver.

7-segment latch/decoder/driver truth table:

| INPUTS | | | | | | | | OUTPUTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **RBI** | **LD** | **B1** | **Ph *** | **D** | **C** | **B** | **A** | **RBO** | **a** | **b** | **c** | **d** | **e** | **f** | **g** | **DISPLAY** |
| X | X | 1 | 0 | X | X | X | X | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| X | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| X | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| X | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| X | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| X | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| X | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| X | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| X | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| X | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 9 |
| X | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| X | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| X | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| X | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| X | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BLANK |
| X | 0 | 0 | 0 | X | X | X | X | | | | | ** | | | | ** |
| † | † | † | † | | | † | | † | | | | Inverse of Output Combinations Above | | | | Display as above |

X Don't care

† Above combinations

*

**

RBO=RBI • (ABCD)

# 7.2.88 4555 (Dual 1-of-4 Dec/DEMUX)

The 4555 device is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A0 and A1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs that are active HIGH (O0 to O3).

Decoder/demultiplexer truth table:

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $\overline{E}$ | A0 | A1 | $\overline{O0}$ | $\overline{O1}$ | $\overline{O2}$ | $\overline{O3}$ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | X | X | 0 | 0 | 0 | 0 |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial

# 7.2.89 4556 (Dual 1-of-4 Dec/DEMUX)

This device contains two independent 1-of-4 decoders/demultiplexers.

Decoders/demultiplexer truth table:

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $\overline{E}$ | A0 | A1 | $\overline{O0}$ | $\overline{O1}$ | $\overline{O2}$ | $\overline{O3}$ |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | X | X | 1 | 1 | 1 | 1 |

# 7.2.90 4585 (4-bit Comparator)

The 4585 device is a 4-bit magnitude comparator that compares two 4-bit words (A and B), whether they are “less than”, “equal to”, or “greater than”. Each word has four parallel inputs (A0 to A3 and B0 to B3).

4-bit comparator truth table:

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| **A3, B3** | **A2, B2** | **A1, B1** | **A0, B0** | **IA>B** | **IA<B** | **IA=B** | **OA>B** | **OA<B** | **OA=B** |
| $A_3>B_3$ | X | X | X | 1 | X | X | 1 | 0 | 0 |
| $A_3<B_3$ | X | X | X | X | X | X | 0 | 1 | 0 |
| $A_3=B_3$ | $A_2>B_2$ | X | X | 1 | X | X | 1 | 0 | 0 |
| $A_3=B_3$ | $A_2<B_2$ | X | X | X | X | X | 0 | 1 | 0 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1>B_1$ | X | 1 | X | X | 1 | 0 | 0 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1<B_1$ | X | X | X | X | 0 | 1 | 0 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0>B_0$ | 1 | X | X | 1 | 0 | 0 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0<B_0$ | X | X | X | 0 | 1 | 0 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | X | 0 | 1 | 0 | 0 | 1 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | 1 | 0 | 0 | 1 | 0 | 0 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | X | 1 | 0 | 0 | 1 | 0 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | X | 1 | 1 | 0 | 1 | 1 |
| $A_3=B_3$ | $A_2=B_2$ | $A_1=B_1$ | $A_0=B_0$ | 0 | 0 | 0 | 0 | 0 | 0 |

1 = HIGH state (the more positive voltage)
0 = LOW state (the less positive voltage)
X = state is immaterial

# 7.3 Tiny Logic

Tiny Logic is a line of single function digital CMOS chips which are intended for applications which require only a single gate to complete a design.

## 7.3.1 NC7S00

This device contains a single 2-input NAND gate.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 7.3.2 NC7S02

This device contains a single 2-input NOR gate.

Logic function:

$$Y = \overline{A+B}$$

NOR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

## 7.3.3 NC7S04

This device contains a single inverter.

Logic function:

$$Y = \overline{A}$$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 7.3.4 NC7S08

This device contains a single 2-input AND gate.

Logic function:

$$Y = AB$$

AND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## 7.3.5 NC7S32

This device contains a single 2-input OR gate.

Logic function:

$$Y = A+B$$

OR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

## 7.3.6 NC7S86

This device contains a single 2-input exclusive-OR gate.

Exclusive-OR gate truth table:

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## 7.3.7 NC7ST00

This device contains a single 2-input NAND gate.

Logic function:

$$Y = \overline{AB}$$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 7.3.8 NC7ST02

This device contains a single 2-input NOR gate.

Logic function:

$$Y = \overline{A+B}$$

NOR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

## 7.3.9 NC7ST04

This device contains a single inverter.

Logic function:

$$Y = \overline{A}$$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 7.3.10 NC7ST08

This device contains a single 2-input AND gate.

Logic function:

$$Y = AB$$

AND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## 7.3.11 NC7ST32

This device contains a single 2-input OR gate.

Logic function:

$Y = A+B$

OR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

## 7.3.12 NC7ST86

This device contains a single 2-input exclusive-OR gate.

Exclusive-OR gate truth table:

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## 7.3.13 NC7SU04

This device contains a single unbuffered inverter.

Logic function:

$Y = \overline{A}$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 7.3.14 NC7SZ00

This device contains a single UHS (ultra high-speed) 2-input NAND gate.

Logic function:

$$Y = \overline{AB}$$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 7.3.15 NC7SZ02

This device contains a single UHS (ultra high-speed) 2-input NOR gate.

Logic function:

$$Y = \overline{A+B}$$

NOR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

## 7.3.16 NC7SZ04

This device contains a single UHS (ultra high-speed) inverter.

Logic function:

$$Y = \overline{A}$$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 7.3.17 NC7SZ05

This device contains a single UHS (ultra high-speed) inverter with open drain output.

Logic function:

$$Y = \overline{A}$$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

## 7.3.18 NC7SZ08

This device contains a single UHS (ultra high-speed) 2-input AND gate.

Logic function:

$$Y = AB$$

AND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

## 7.3.19 NC7SZ125

This device contains a single UHS (ultra high-speed) buffer with 3-state output.

BUFFER gate truth table:

| $\overline{A}$ | Y |
|---|---|
| $\overline{0}$ | 0 |
| $\overline{1}$ | 1 |

## 7.3.20 NC7SZ126

This device contains a single UHS (ultra high-speed) buffer with 3-state output.

BUFFER gate truth table:

| $\overline{A}$ | Y |
|---|---|
| $\overline{0}$ | 0 |
| $\overline{1}$ | 1 |

## 7.3.21 NC7SZ32

This device contains a single UHS (ultra high-speed) 2-input OR gate.

Logic function:

$$Y = A+B$$

OR gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

## 7.3.22 NC7SZ38

This device contains a single UHS (ultra high-speed) 2-input NAND gate with open drain output.

Logic function:

$Y = \overline{AB}$

NAND gate truth table:

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

## 7.3.23 NC7SZ86

This device contains a single UHS (ultra high-speed) 2-input exclusive-OR gate.

Exclusive-OR gate truth table:

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# 7.3.24 NC7SZU04

This device contains a single UHS (ultra high-speed) unbuffered inverter.

Logic function:

$$Y = \overline{A}$$

INVERTER gate truth table:

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

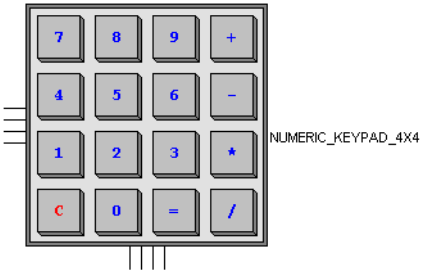
# Chapter 8
# Advanced Peripherals

The devices documented in this chapter are not available in all versions of Multisim.

## 8.1 Keypads

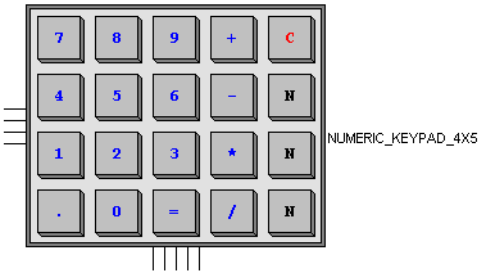
These devices are not available in all versions of Multisim.

### 8.1.1 4X4 Numeric Keypad



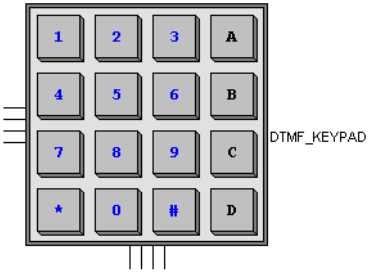

This device is a 4X4 numeric keypad. While the circuit is simulating, press a key on your keyboard to “press” the same key on this device. You can also hover your cursor over the desired key on the keypad and click to “press” the key.

## 8.1.2 4x5 Numeric Keypad




This device is a 4X5 numeric keypad. While the circuit is simulating, press a key on your keyboard to “press” the same key on this device. You can also hover your cursor over the desired key on the keypad and click to “press” the key.

## 8.1.3 DTMF Keypad




This device is a Dual Tone Multi-Frequency keypad. The DTMF keypad is laid out in a 4×4 matrix, with each row representing a low frequency, and each column representing a high frequency.

While the circuit is simulating, press a key on your keyboard to “press” the same key on this device. You can also hover your cursor over the desired key on the keypad and click to “press” the key.

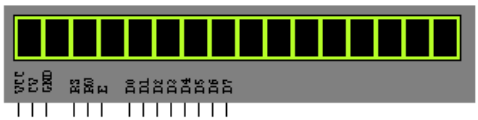
# 8.2 LCDs

This feature is not available in all versions of Multisim.

## 8.2.1 LCD Displays

This feature is not available in all versions of Multisim.

The **LCDS** component **Family** contains a number of LCDs similar to the following:




The number of characters available for display changes depending on the LCD selected (e.g., 16x1 in the LCD shown above). The controller for these devices is based on the Hitachi 44780 LCD controller.

Pins on the LCDs are:

- **VCC** — Supply Voltage
- **CV** — Contrast Voltage
- **GND** — Ground
- **RS** — Instruction/Register Select
- **RW** — Read/Write LCD Registers
- **E** — Clock. Initiates data transfer within the LCD
- **D0** to **D7** — Data I/O pins.

➢ To set the LCD's character set and trigger type:

1. Double-click on the placed LCD and click the **Value** tab.
2. Adjust the following as desired:
   - **Base Character Set** — choose one of: 0 for Hitachi; 1 for Intel/Motorola
   - **Character Subset** — if you chose 1 for the **Base Character Set**, choose one of: 28 for European; 29 for Katakana; 30 for Cyrillic; 31 for Hebrew
   - **Trigger Type** — choose 0 for High Level; 1 for Falling Edge.
3. Click **OK** to close the dialog box and save the changes to the device.

**Instruction Set**

| RS | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 5 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | Pins |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Clear display |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Return Cursor and LCD to home positon |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | ID | S | Set Cursor Move Direction |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | * | Enable Display/Cursor |
| 0 | 0 | 0 | 0 | 0 | 1 | SC | RL | * | * | Move Cursor/Shift Display |
| 1 | 0 | D | D | D | D | D | D | D | D | Write a Character to the Display at Current Cursor Position |

* - Bit can be either “1” or “0”.

**Set Cursor Move Direction:**

ID - Increment the cursor after each byte written to display if set.

S - Shift display when byte written to display.

**Enable Display/Cursor:**

D - Turn display on (1)/off (0).

C - Turn cursor on (1)/off (0).

**Move Cursor/Shift Display:**

SC - Display shift on (1)/off (0).

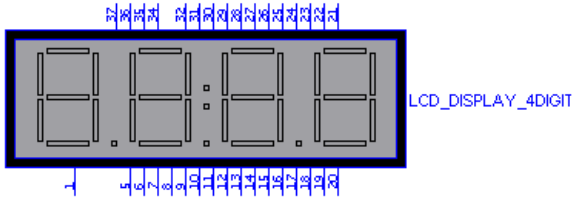
RL - Direction of shift right (1)/ left (0).

**Write a Character to the Display:**

D - Data.

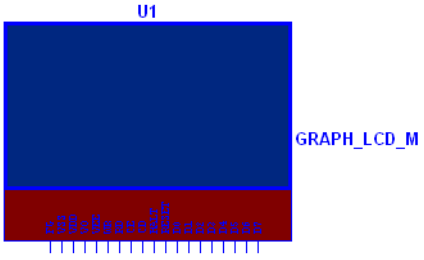
## 8.2.2 Four Digit LCD Display

This feature is not available in all versions of Multisim.




This device is a four-digit LCD display.

## 8.2.3 Graphic LCD Display




This device emulates the behavior of a graphical LCD and controller. The controller is based on the Toshiba T6963C controller.

***Note*** For a demonstration of this part, refer to the Multisim MCU Module chapter of *Getting Started with NI Circuit Design Suite*.

The following information is included in this section:

- Features
- Pin Descriptions
- Basic Commands

For more detailed information on the T6963C controller, including datasheets, National Instruments recommends that you check the internet.

## Features

- Supports three modes: Graphics, Text, Graphic + Text
- Up to 256 x 256 pixel display resolution
- Displays in two colors
- Display columns in Text mode: 32 - 50
- Display lines in Text mode: 2 - 32
- Font Width: 5, 6, 7, 8
- Font Height: 8
- Maximum number of the characters is 256; 0 – 127 in ROM area (character code 0101)
- 20 pins with 8 data pins (Pin definition is based on Futurlec T6963 LCD)
- Command system based on Toshiba T6963C
- Single-scan memory mode
- Internal memory RAM: 12kB (minimum required size, T6963 allows maximum of 64 kB)

## Pin Descriptions

| Pin Name | No. | I/O | Functions |
|---|---|---|---|
| FG | 1 | — | Frame Ground |
| VSS | 2 | — | GND (0 V) |
| Vdd | 3 | — | Supply Voltage for Logic (5.0 V) |
| VO | 4 | — | Operating Voltage for LCD (-15.0 V) |
| Vee | 5 | — | Supply Voltage for LCD (-15.0 V) |
| WR | 6 | Input | Data Write. Write data into T6963C when WR = L. |
| RD | 7 | Input | Data Read. Read data from T6963C when RD = L. |
| CE | 8 | Input | Chip Enable for T6963C. CE must be L when CPU communicates with T6963C. |
| C / D | 9 | Input | WR = L ····· C / D = H: Command Write<br>C / D = L: Data Write<br>RD = L ····· C / D = H: Status Read<br>C / D = L: Data Read |
| HALT | 10 | Input | H ····· Normal, L ····· Stops the oscillation of the clock |
| RESET | 11 | Input | H Normal (T6963C has internal pull-up resistor)<br>L Initialize T6963C. Text and graphic have addresses and text and graphic area settings are retained. |

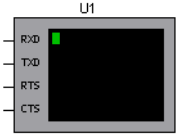
| Pin Name | No. | I/O | Functions |
|---|---|---|---|
| D0 to D7 | 12-19 | I/O | Data I / O pins between CPU and T6963C (D7 is MSB) |
| NC | 20 | | No Connect |

## Basic Commands

| Command | Code | D1 | D2 | Function | Hex |
|---|---|---|---|---|---|
| REGISTERS SETTING | 00100001<br>00100010<br>00100100 | TCX address<br>Data<br>Low address | TCY addr.ess<br>00H<br>High addr.ess | Set Cursor Pointer<br>Set Offset Register<br>Set Address Pointer | 21H<br>22H<br>23H |
| SET CONTROL WORD | 01000000<br>01000001<br>01000010<br>01000011 | Low address<br>Columns TA<br>Low address<br>Columns GA | Low address<br>00H<br>Low address<br>00H | Set Text Home Address<br>Set Text Area<br>Set Graphic Home Address<br>Set Graphic Area | 40H<br>41H<br>42H<br>43H |
| MODE SET | 1000X000<br>1000X001<br>1000X011<br>1000X100<br>10000XXX<br>10001XXX | --<br>--<br>--<br>--<br>--<br>-- | --<br>--<br>--<br>--<br>--<br>-- | OR mode<br>EXOR mode<br>AND mode<br>Text Attribute mode<br>Internal CG ROM mode<br>External CG RAM mode | 8*H |
| DISPLAY MODE | 10010000<br>1001XX10<br>1001XX11<br>100101XX<br>100110XX<br>100111XX | --<br>--<br>--<br>--<br>--<br>-- | --<br>--<br>--<br>--<br>--<br>-- | Display off<br>Cursor on, blink off<br>Cursor on, blink on<br>Text on, graphic off<br>Text off, graphic on<br>Text on, graphic on | 9*H |
| CURSOR PATTERN SELECT | 10100000<br>10100001<br>10100010<br>10100011<br>10100100<br>10100101<br>10100110<br>10100111 | --<br>--<br>--<br>--<br>--<br>--<br>--<br>-- | --<br>--<br>--<br>--<br>--<br>--<br>--<br>-- | 1-line cursor<br>2-line cursor<br>3-line cursor<br>4-line cursor<br>5-line cursor<br>6-line cursor<br>7-line cursor<br>8-line cursor | A*H |
| DATA AUTO READ / WRITE | 10110000<br>10110001<br>10110010 | --<br>--<br>-- | --<br>--<br>-- | Set Data Auto Write<br>Set Data Auto Read<br>Auto Reset | B0H<br>B1H<br>B2H |

| Command | Code | D1 | D2 | Function | Hex |
|---|---|---|---|---|---|
| DATA READ/ WRITE | 11000000 | Data | -- | Data Write and Increment ADP | C0H |
| | 11000001 | -- | -- | Data Read and Increment ADP | C1H |
| | 11000010 | Data | -- | Data Write and Decrement ADP | C2H |
| | 11000011 | -- | -- | Data Read and Decrement ADP | C3H |
| | 11000100 | Data | -- | Data Write and Nonvariable ADP | C4H |
| | 11000101 | -- | -- | Data Read and Nonvariable ADP | C5H |
| Screen Peek | 11100000 | -- | -- | Screen Peek | E0H |
| Screen Copy | 11100001 | -- | -- | Screen Copy | E1H |
| BIT SET / RESET | 11110XXX | -- | -- | Bit Reset | F*H |
| | 11111XXX | -- | -- | Bit Set | |
| | 1111X000 | -- | -- | Bit 0 (LSB) | |
| | 1111X001 | -- | -- | Bit 1 | |
| | 1111X010 | -- | -- | Bit 2 | |
| | 1111X011 | -- | -- | Bit 3 | |
| | 1111X100 | -- | -- | Bit 4 | |
| | 1111X101 | -- | -- | Bit 5 | |
| | 1111X110 | -- | -- | Bit 6 | |
| | 1111X111 | -- | -- | Bit 7 (MSB) | |

# 8.3 Virtual Terminal




This device interfaces with the serial port that is used in conjunction with Multisim MCU's microcontroller devices.

It includes a virtual terminal window where you can type characters on your keyboard. When a simulation is running, the virtual terminal does not normally display the characters that you type into it. The terminal just sends the characters that are typed into its window through its TxD pin at the baud rate that it is set to in its properties dialog. The terminal displays any characters that it receives through its RxD pin.

- To set the speed for this device:
  1. Double-click on the placed virtual terminal and click on the **Value** tab.
  2. Enter the desired speed in the **Baud Rate (bps)** field.
  3. Click **OK** to close the dialog.

## Displaying Elements of the Virtual Terminal

- To show/hide the elements of the virtual terminal:
  1. Double-click on the placed virtual terminal to display its properties dialog box and click on the **Display** tab.
  2. Enable the **Virtual Terminal Window** checkbox as desired and click on the **OK** button.

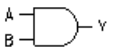
# Chapter 9
# Misc. Digital Components

## 9.1 TIL Components

A number of TIL components are included in Multisim, including:


- "AND Gate" on page 9-1
- "OR Gate" on page 9-2
- "NOT Gate" on page 9-3
- "NOR Gate" on page 9-3
- "NAND Gate" on page 9-4
- "XOR Gate (Exclusive OR)" on page 9-4
- "XNOR Gate (Exclusive NOR)" on page 9-5
- "Tristate Buffer" on page 9-6
- "Buffer" on page 9-6
- "Schmitt Trigger" on page 9-7
- "Digital Pulldown" on page 9-8
- "Digital Pull-up" on page 9-8
- "Digital State Machine" on page 9-8
- "BCD_7SEG_DCD" on page 9-9
- "Parity Generator/Checker" on page 9-9
- "Quad 2-to-1 Data Sel/MUX" on page 9-9
- "Digital Frequency Divider" on page 9-10


### 9.1.1 AND Gate




This component has a high output only when all inputs are high.

AND gate truth table:

| a | b | y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Boolean Expression:

$$y = a * b$$

$$y = a \& b$$

## 9.1.2 OR Gate




This component has a high output when at least one input is high.

OR gate truth table:

| a | b | y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Boolean Expression:

$$y = a + b$$

$$y = a \mid b$$

## 9.1.3 NOT Gate




This component inverts, or complements, the input signal. If the input is high, the output is low, and vice versa.

NOT gate truth table:

| a | y |
|---|---|
| 0 | 1 |
| 1 | 0 |

Boolean Expression:

$y = a'$

$y = \overline{a}$

## 9.1.4 NOR Gate




This component is a NOT OR, or an inverted OR gate. Its output is high only when all the inputs are low. Using a NOR gate is the same as having a NOT gate at the output of an OR gate.

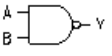
NOR gate truth table:

| a | b | y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Boolean Expression:

$$y = (a + b)'$$
$$y = \overline{a + b}$$

## 9.1.5 NAND Gate




This component is a NOT AND, or inverted AND, gate. Its output is low only when all inputs are high. Using a NAND gate is the same as having a NOT gate at the output of an AND gate.

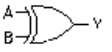
NAND gate truth table:

| a | b | y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Boolean Expression:

$$y = (a * b)'$$
$$y = \overline{a * b}$$

## 9.1.6 XOR Gate (Exclusive OR)




This component has a high output when an odd number of inputs (1, 3, 5, etc.) is high. An even number of high inputs generates a low output.

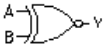
XOR gate truth table:

| a | b | y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Boolean Expression:

$$y = a \oplus b$$
$$y = a'b' + ab'$$

## 9.1.7 XNOR Gate (Exclusive NOR)




This component has a high output when an even number of inputs (2, 4, 6, etc.) is high. An odd number of high inputs generates a low output.

XNOR gate truth table:

| a | b | y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Boolean Expression:

$$y = \overline{a \oplus b}$$
$$y = \left(a'b + ab'\right)'$$

## 9.1.8 Tristate Buffer




This component is a non-inverting buffer with a three-state output. It has a greater fan-out and offers a high-current source and sink capability for driving high-current loads. The buffer has an active-high enable input.

If the device is not “enabled”, then the buffer output goes into a high-impedance (Z) state. In this state, the output pin is effectively disconnected from the rest of the circuit. Thus, the buffer is useful for circuits where outputs from different digital devices meet at the same node.

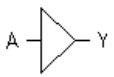
Truth table:

| input | enable input | output |
|---|---|---|
| 1 | 1 | 1 |
| 0 | 1 | 0 |
| X | 0 | Z |

where Z is a high-impedance state

***Note*** When using a tristate buffer use the Models tab of the Circuit/Component Properties dialog box. Select the LS-BUF or LS-OC-BUF (OC = Open-collector) model if the buffer is being used as a TTL device. Select HC-BUF or HC-OD-BUF if the tristate buffer is being used as a CMOS device. Otherwise, by default, the tristate buffer will behave as a regular digital device without any high-current capabilities.

## 9.1.9 Buffer




This component is a non-inverting buffer. It has a greater fan-out and offers a high-current source and sink capability for driving high-current loads.

Truth table:

| input | output |
|---|---|
| 1 | 1 |
| 0 | 0 |

***Note*** When using a buffer, set it up using the Models tab of the Circuit/Component Properties dialog box. Select the LS-BUF or LS-OC-BUF model if the buffer is being used as a TTL device. Select HC-BUF or HC-OD-BUF if the buffer is being used as a CMOS device. Otherwise, by default, the buffer will behave as a regular digital device without any high-current capabilities.

## 9.1.10 Schmitt Trigger




This component is a type of comparator with hystereses that produces uniform-amplitude output pulses from a random-amplitude input signal. It has applications in pulse systems, for example, converting a sine wave into a square wave.

Characteristic Operation:

The Schmitt trigger outputs:

0 if the voltage is rising and $V_{in} > V_{+g}^{+}$

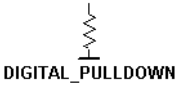
1 if the voltage is falling and $V_{in} < V_{+g}^{-}$

where:

$V_{+g}^{+} = 1.6\ V\ (V_{ih})$

$V_{+g}^{-} = 0.9\ V\ (V_{il})$

## 9.1.11 Digital Pulldown



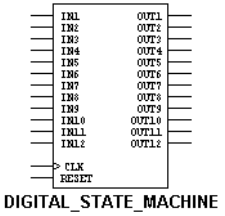

A digital pull-down resistor emulates the behavior of an analog resistance value tied to a low voltage level.

## 9.1.12 Digital Pull-up



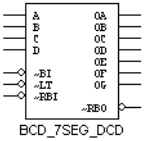

A digital pull-up resistor emulates the behavior of an analog resistance value tied to a high voltage level.

## 9.1.13 Digital State Machine




The digital state machine's model can be configured to act as most types of counter or clocked combinational logic blocks. Use this device to replace large digital schematics.

## 9.1.14 BCD_7SEG_DCD




This device is a generic BCD to 7 -segment decoder, which is used to convert the output of a BCD counter into a form that will drive a 7-segment display.

## 9.1.15 Parity Generator/Checker

This 9-bit (8 data bits plus 1 parity bit) parity generator/checker features odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications.

Parity generator/checker truth table:

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| S OF H's AT A THRU H | EVEN | ODD | S EVEN | S ODD |
| Even | 1 | 0 | 1 | 0 |
| Odd | 1 | 0 | 0 | 1 |
| Even | 0 | 1 | 0 | 1 |
| Odd | 0 | 1 | 1 | 0 |
| X | 1 | 1 | 0 | 0 |
| X | 0 | 0 | 1 | 1 |

## 9.1.16 Quad 2-to-1 Data Sel/MUX

This device contains inverters and drivers to supply full on-chip data selection to the four output gates. It presents inverted data to minimize propagation delay time.

A 4-bit word is selected from one of two sources and is routed to the four outputs.

Data selector/multiplexer truth table:

| STROBE | SELECT | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | $\overline{A}$/B | A | B | Y |
| 1 | X | X | X | 1 |
| 0 | 0 | 0 | X | 1 |
| 0 | 0 | 1 | X | 0 |
| 0 | 1 | X | 0 | 1 |
| 0 | 1 | X | 1 | 0 |

## 9.1.17 Digital Frequency Divider

This device is a programmable step-down divider which accepts an arbitrary divisor, a duty-cycle term and an initial count value. The generated output is synchronized to the rising edges of the input signal. Rise and fall delay on the outputs are independently specifiable.

# 9.2 VHDL

VHDL (Very High Speed Integrated Circuit (VHSIC) Hardware Description Language) is designed to describe the behavior of complex digital devices. For this reason it is referred to as a "behavioral level" language; it can use behavioral level models (instead of transistor/gate level, like SPICE) to describe the behavior of these devices.

The VHDL **Family** contains a number of VHDL-modeled components, including:

- Quad NAND gates
- Quad NOR gates
- Quad AND gates
- Inverters
- Buffers
- Counters
- Drivers
- MUXs
- Flip-flops
- SRAM.

***Note*** For details on MultiVHDL , Electronic Workbench's VHDL simulation software, refer to the *Multisim User Guide*, or the *MultiVHDL 8 User Guide*.

# 9.3 Memory

A number of EPROM and RAM memory devices are included in Multisim. In addition to the components that contain footprint and model information (for simulation), there are several that include only the footprint, for PCB layout.

# 9.4 Line Receiver

Line receivers are devices which are used in applications such as a bridge between analog signal and digital signals such as RS232 interfaces, or long signal runs over cables. The line receivers are placed at the receiving end of the application before the digital circuits.

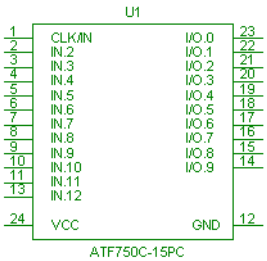
# 9.5 Line Driver

Line drivers are devices which are used in applications such as a bridge between analog signal and digital signals such as RS232 interfaces, or long signal runs over cables. The line drivers are placed at the transmitting end of the application after the digital circuits.

# 9.6 Line Transceiver

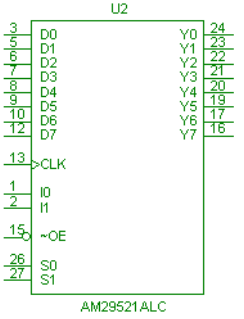
Line transceivers are devices, which are used in applications such as a bridge between analog signal and digital signals such as RS232 interfaces, or long signal runs over cables. The line transceivers are placed between the digital circuits.

# 9.7 CPLDs



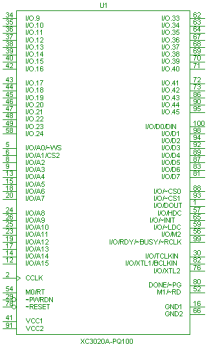
A number of CPLDs (Complex Programmable Logic Devices) are included that have symbols for layout purposes. These also have footprint, but no model information.

# 9.8 DSP Devices



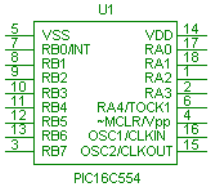

A number of DSPs (Digital Signal Processors) are included that have symbols for layout purposes. These also have footprint, but no model information.

# 9.9 FPGA Devices



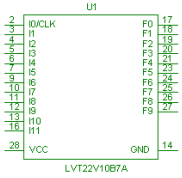

A number of FPGAs (Field Programmable Gate Arrays) are included that have symbols for layout purposes. These also have footprint, but no model information.

# 9.10 Microcontrollers



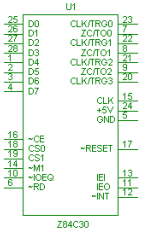

A number of microcontrollers are included that have symbols for layout purposes. These also have footprint, but no model information.

# 9.11 Programmable Logic Devices




A number of PLDs (Programmable Logic Devices) are included that have symbols for layout purposes. These also have footprint, but no model information.

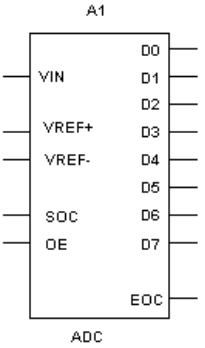
# 9.12 Microprocessors




A number of microprocessors are included that have symbols for layout purposes. These also have footprint, but no model information.

# Chapter 10
# Mixed Components

## 10.1 ADC DAC




An ADC is a special type of encoder that converts the input analog voltage to an equivalent output digital word.

### 10.1.1 Characteristic Equation

The $V_{in}$ input is the analog voltage input. The voltage at $V_{ref+}$ and $V_{ref}$- pins set up the full-scale voltage. The full-scale voltage is given by:

$$V_{fs} = V_{ref+} - V_{ref-}$$

To start the conversion, the SOC pin should be driven high. This pulls the EOC pin low, signifying that a conversion is taking place. The conversion takes 1 µS to complete and the EOC pin is pulled high when it is completed. The output digital data is now available at pins

D0 through D7. These are tri-stated outputs pins which may be enabled by pulling the OE pin high.

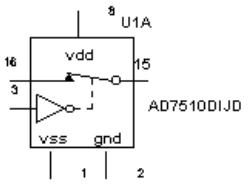
The output at the end of the conversion process is the digital equivalent of the analog input voltage. The discrete value corresponding to the quantized level of input voltage is given by:

$$\frac{input\ voltage * 256}{V_{fs}}$$

Note that the output described by this formula is not a continuous function of input voltage. The discrete value is then encoded into the binary digital form at pins D0 through D7. The binary output is thus given by:

$$BIN\left[\frac{input\ voltage * 256}{V_{fs}}\right]$$

# 10.2 Analog Switch



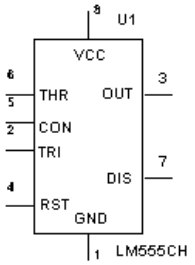

This switch is a resistor that varies logarithmically between specified values of a controlling input voltage. Note that the input is not internally limited. Therefore, if the controlling signal exceeds the specified Coff or Con values, the resistance may become excessively large or small.

The voltage controlled switch has a function similar to that performed by a mechanical On/Off switch except that the On/Off conditions are selected by a control voltage.

When the control voltage is below a selected value, the switch is off and the input and output signals are disconnected.

When the control voltage is above the selected value, the switch is on and the input and output signals are connected.

# 10.3 Timer




The 555 timer is an IC chip that is commonly used as an astable multivibrator, a monostable multivibrator or a voltage-controlled oscillator. The 555 timer consists basically of two comparators, a resistive voltage divider, a flip-flop and a discharge transistor. It is a two-state device whose output voltage level can be either high or low. The state of the output can be controlled by proper input signals and time-delay elements connected externally to the 555 timer.

## 10.3.1 Model

The resistive voltage divider is used to set the voltage comparator levels. All three resistors are of equal value. The upper comparator has a reference voltage of 2/3 $V_{cc}$ and the lower comparator has a reference of 1/3 $V_{cc}$. The comparator's output controls the state of the flip-flop and hence the output. When the trigger voltage goes below 1/3 $V_{cc}$, the output of the lower comparator goes high, and the flip-flop sets. The output thus jumps to a high level. The threshold input is normally connected to an external RC timing network. When the external voltage exceeds 2/3 $V_{cc}$, the upper comparator's output goes high and resets the flip-flop, which in turn switches the output back to the low level. When the device output is low, the discharge transistor, Q, is turned on and provides a path for the discharge of the external timing capacitor.

This basic operation allows the timer to be configured with external components as an oscillator, a monoshot or a time-delay element.

# 10.4 Mono Stable

This component produces an output pulse of a fixed duration in response to an “edge” trigger at its input. The length of the output pulse is controlled by the timing RC circuit connected to the monostable multivibrator.

## 10.4.1 Model

A monostable multivibrator has two digital inputs: A1 and A2. The multivibrator can be triggered by a positive edge of digital signal at A1 or a negative edge at A2. Once triggered, it ignores further inputs.

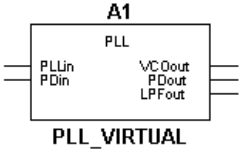
An RC combination connected to RT/CT and CT pins controls the duration of the pulse produced by the monostable at Q. A complementary output is produced at W.

- To operate the monostable, the following connections may be used:
  - Connect a series resistor (R) and capacitor (C) to the CT input.
  - Connect the junction of the R and C to the RT/CT.
  - Connect $V_{CC}$ to a voltage source.

The output Q will give a pulse of duration 0.0693*R*C when either a positive clock edge is given to A1 or a negative edge is given to A2.

The threshold voltage (at which triggering starts) can be changed by modifying the model.

# 10.5 Phase-Locked Loop




This component models the behavior of a phase-locked loop circuit, which is a circuit that contains an oscillator whose output phase and frequency are steered to keep it synchronized with an input reference signal.

A phase-locked loop circuit is composed of three functional blocks: a phase detector, a low-pass filter and a voltage-controlled oscillator (VCO). The phase detector behaves as an analog multiplier. It outputs a DC voltage which is a function of the phase difference between the

input reference signal and the VCO output signal. The output of the phase detector is input to the low-pass filter, which removes the high-frequency noise and outputs a DC voltage. The VCO converts the DC voltage into its corresponding frequency signal.

## 10.5.1 Characteristic Equation

The phase detector is modeled by:

$$V_d = K_d * \sin(\varphi_i - \varphi_o)$$

$$\varphi_i = 2\pi * \int f_1(t)dt$$

The low-pass filter is modeled by a simple passive RC low-pass filter, that is, a resistor and a capacitor, where R is 3.6 kohm, and:

$$C = \frac{1}{2\pi * f_p * R}$$

The voltage-controlled oscillator (VCO) is modeled by:

$$f_o(t) = f_c + K_o * V_c(t)$$

$$\varphi_o = 2\pi * \int f_o(t)dt$$

where:

$f_i$ = input frequency

$f_p$ = low-pass filter pole location

$f_o$ = VCO output frequency

$f_c$ = VCO free-running frequency

$V_d$ = phase detector output DC voltage

$V_o$ = VCO output voltage

$K_o$ = VCO conversion gain

$K_d$ = phase detector conversion gain

$\varphi_i$ = input signal phase

$\varphi_o$ = VCO output phase

### 10.5.2 Phase-Locked Loop Parameters and Defaults

| Symbol | Parameter name | Default | Unit |
|---|---|---|---|
| *Kd* | Phase detector conversion gain | 0.25 | V/rad |
| *Ko* | VCO conversion gain | 500 | kHz/ V |
| *fc* | VCO free-running frequency | 250 | kHz |
| *fp* | Low-pass filter cut-off frequency | 25 | kHz |
| *Vom* | VCO output amplitude | 1.0 | V |
| -- | PLL Input Offset | 0 | V |
| -- | PD Input Offset | 0 | V |
| -- | VCO Output Offset | 0 | V |

## 10.6 Multivibrators

### 10.6.1 CD4538BC

The CD4538 is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active LOW and prevent triggering while active. The pulse duration and accuracy are determined by external components $R_X$ and $C_X$. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this

reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↓ | ⎍ | ⎍ |
| H | ↑ | H | ⎍ | ⎍ |

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎍ = One LOW Level Pulse
X = Irrelevant

## 10.6.2 SN74121N

This multivibrator has dual negative-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| A1 | A2 | B | Q | $\overline{Q}$ |
| L | X | H | L | H |
| X | L | H | L↑ | H↑ |
| X | X | L | L↑ | H↑ |
| H | H | X | L↑ | H↑ |
| H | ↓ | H | ⎍ | ⎍ |
| ↓ | H | H | ⎍ | ⎍ |
| ↓ | ↓ | H | ⎍ | ⎍ |
| L | X | ↑ | ⎍ | ⎍ |
| X | L | ↑ | ⎍ | ⎍ |

### 10.6.3 SN74123

This DC triggered multivibrator has output pulse duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values. Enough Schmitt hysteresis is provided to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 mV per nanosecond.

### 10.6.4 SN74130N

This DC triggered multivibrator has output pulse duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values.

## 10.7 Frequency Divider

This is an Asynchronous Binary Counter Based Frequency Divider. The amplitude of the square wave output can be defined by the user via the dialog box. This device is ideal for use with the virtual PLL in frequency synthesis applications.

# Chapter 11
# Indicators

## 11.1 Voltmeter




The voltmeter offers advantages over the multimeter for measuring voltage in a circuit. You can use an unlimited number of voltmeters in a circuit and rotate their terminals to suit your layout.

### Resistance (1.0 Ω - 999.99 TW)

The voltmeter is preset to a very high resistance (1 MΩ(+)) which generally has no effect on a circuit. If you are testing a circuit that itself has very high resistance, you may want to increase the voltmeter's resistance to get a more accurate reading. (However, using a voltmeter with very high resistance in a low-resistance circuit may result in a mathematical round-off error.)

### Mode (DC or AC)

The voltmeter can measure DC or AC voltage. In DC mode, any AC component of the signal is eliminated so that only the DC component of the signal is measured. In AC mode, any DC component is eliminated so that only the AC component is measured. When set to AC, the voltmeter displays the root-mean-square (RMS) value of the signal.

### Connecting a Voltmeter

Connect the voltmeter in parallel with the load, attaching the probes to connectors on either side of the load you want to measure. When a circuit is activated and its behavior is simulated, the voltmeter displays the voltage across the test points. (The voltmeter may also display interim voltages before the final steady-state voltage is reached.)

***Note*** If a voltmeter is moved after the circuit has been simulated, activate the circuit again to get a reading.

# 11.2 Ammeter




The ammeter offers advantages over the multimeter for measuring current in a circuit. You can use an unlimited number of ammeters in a circuit and rotate their terminals to suit your layout.

## Resistance (1.0 pΩ - 999.99 W)

The ammeter's resistance is preset to 1 mΩ, which presents little resistance to a circuit. If you are testing a circuit that has low resistance, you can lower the ammeter's resistance even further to get a more precise measurement. (However, using an ammeter with very low resistance in a high-resistance circuit may result in a mathematical round-off error.)

## Mode (DC or AC)

The ammeter is preset to DC mode, which measures only the DC component of a signal. If you want to measure the current from an AC source, change the mode to AC. When set to AC, the ammeter displays the root-mean-square (RMS) value of the alternating signal.

## Connecting an Ammeter

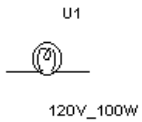
Like a real ammeter, the simulated ammeter must be connected in series at nodes you want to measure. The negative terminal is on the side with the heavy border. If an ammeter is moved after the circuit has been simulated, activate the circuit again to get a reading.

# 11.3 Digital Probe




The probe indicates high (on) or low (off) levels at any point in a digital circuit. It lights up or turns off as the circuit is running, and is available in a number of colors.

# 11.4 Lamp




The lightbulb is an ideal, nonlinear resistive component that dissipates energy in the form of light. It has two rated values, maximum power ($P_{max}$) and maximum voltage ($V_{max}$). $P_{max}$ is measured in watts, from mW to kW. $V_{max}$ is measured in volts, from mV to kV. A bulb will burn out if the voltage across it exceeds $V_{max}$. At that point, the power dissipated in the bulb exceeds $P_{max}$.

## 11.4.1 Time-Domain and AC Frequency Models

The bulb is modeled by a resistor, $R$.

$$R = \frac{V_{\max}^2}{P_{\max}} \quad if \quad |V_{ab}| \le V_{\max}$$

$$R = \infty \quad if \quad |V_{ab}| > V_{\max}$$

The bulb is lit if

$$\frac{V_{\max}}{2} < |V_{ab}| \le V_{\max}$$

where:

$V_{max}$ = the maximum voltage that can be applied across the bulb.

$P_{max}$ = the maximum power that can be dissipated by the bulb.

For AC circuits, $V_{max}$ is the peak value of the applied voltage, not its RMS value.

# 11.5 Hex Displays

## 11.5.1 Seven-Segment Display

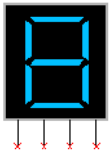



The seven-segment display actively shows its state while the circuit is running. The seven terminals (left to right, respectively) control segments a to g. By giving the proper binary-digit inputs to segments a to g, you can display decimal numbers from 0 to 9 and letters A to F.

Truth table:

| a | b | c | d | e | f | g | Digit displayed |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | none |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 9 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | A |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | b |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | C |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | d |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | E |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | F |

## 11.5.2 Decoded Seven-Segment Display

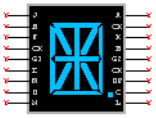


This display indicates its current state by displaying hexadecimal digits—numerals 1 to 9 and letters A to F. It is easier to use than the regular seven-segment display because it is already decoded. Each hexadecimal digit is displayed when its 4-bit binary equivalent is received as input, as shown in the truth table below.

Truth table:

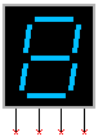
| a | b | c | d | Digit displayed |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | A |
| 1 | 0 | 1 | 1 | b |
| 1 | 1 | 0 | 1 | C |
| 1 | 1 | 0 | 0 | d |
| 1 | 1 | 1 | 0 | E |
| 1 | 1 | 1 | 1 | F |

## 11.5.3 Alpha-Numeric Display



This device is a 15-segment LED alpha-numeric display, which displays text or numeric digits. Both common-anode and common-cathode displays are available.

## 11.5.4 DCD Hex Display



This device is a 7-segment digital hex display.

## 11.5.5 Plus or Minus 1 LED Display




This device is a plus or minus 1 LED display with a decimal point.

## 11.5.6 Two Digit 7-Segment Display




This is a two-digit seven-segment hex display. Both common-anode and common-cathode displays are available.

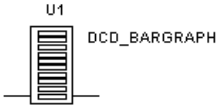
## 11.5.7 Duplexed Seven-Segment Display

This device is a duplexed 7-segment display with decimal point.

➢ To change “on current”:

1. Double-click on the placed device and click on the **Value** tab.
2. Change the value in the **On Current (Ion)** field as desired and click **OK** to close the dialog.

# 11.6 Bargraphs




This display is an array of 10 LEDs arranged side by side. This component may be used to indicate visually the rise and fall of a voltage. The voltage to be measured needs to be decoded into levels using comparators which are used to drive each individual LED.

The terminals on the left side of the display are anodes and the terminals on the right are cathodes. Each LED lights up when the turn-on current, $I_{on,}$ flows through it. You can change the voltage drop in the Value tab of the Circuit/Component Properties dialog box.

### Bargraph Display Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *Vf* | Forward voltage drop | 2 | V |
| *If* | Forward current at which Vf is measured | 0.03 | A |
| *Ion* | Forward current | 0.01 | A |

## 11.6.1 Decoded Bargraph Display

This display consists of 10 LEDs arranged side by side, just like the regular bargraph display. The difference is that the decoded bargraph display already has the decoding circuitry built-in so that it only requires the voltage to be measured as an input to the display. The circuitry inside decodes the voltage and lights up the appropriate number of LEDs, depending on the voltage level.

The decoded bargraph display also offers a very high resistance to the input voltage. The minimum voltages required for the lowest LED and the highest LED are set in the Value tab of the Circuit/Component Properties dialog box. The voltage at which each LED (from lowest to highest) lights up is given by the formula:

$$V_{on} = V_l + \frac{(V_h - V_l)}{9} * (n - 1)$$

where:

n = 1, 2, ..., 10 (the number of the LED)

Other terms in this formula are defined in the table below.

### Decoded Bargraph Display Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *Vl* | Minimum turn-on voltage required for the lowest segment | 1 | V |
| *Vh* | Minimum turn-on voltage required for the highest segment | 10 | V |

# 11.7 Buzzer/Sonalert Buzzer




This component uses the computer's built-in speaker to simulate an ideal piezoelectric buzzer. A piezoelectric buzzer sounds at a specific frequency when the voltage across its terminals exceeds the set voltage.

The buzzer is simulated as a single resistor whose resistance value is dependent on the buzzer's rated voltage and the current. It beeps when the voltage across its terminals exceeds its voltage rating, $V_{rated}$.

Buzzer resistance

$$r = \frac{V_{rated}}{i_{rated}}$$

Beeps when

$$V_{ab} \geq V_{rated}$$

# Chapter 12
# Power

## 12.1 SMPS Transient Virtual

This component family contains a variety of transient switched-mode power supplies (SMPS).

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

For more information about the components described in the following sections, refer to the Switch-Mode Power Supply SPICE Cookbook, McGraw-Hill, 2001.

### 12.1.1 PWMCM

This is a generic current mode PWM controller. The PWMCM uses an error voltage to directly control the peak current of the power switch. The error voltage is derived in the feedback system from the error amplifier that amplifies the difference between the output voltage and the reference voltage.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT | PWM signal Output (MOSFET switch signal) |
| 2 | GND | Ground |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |

| Pin No. | Pin Name | Description |
|---|---|---|
| 5 | ISENSE | Switch current sensing |
| 6 | VOSC | Oscillator ramp signal output (provided for ramp compensation purposes) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| RAMP | Ramp amplitude for compensation |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.2 PWMVM

This device is a generic voltage mode PWM controller. In the PWMVM, an error voltage is compared to a sawtooth ramp to control the duty cycle of the power switch. The higher the error voltage, the longer the duty cycle (i.e., the on-time of power switch). The error voltage is derived in a feedback system from the error amplifier that amplifies the difference between the output voltage and the reference voltage.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT | PWM signal Output (MOSFET switch signal) |
| 2 | GND | Ground |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing (for current limit) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| IMAX | Maximum voltage on (external) current sensing resistor |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |

| Parameter | Description |
|---|---|
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.3 PUSH_VM

The PUSH_VM is a generic model for Voltage Mode Push-Pull PWM controllers. Push-pull is an isolated version of a buck converter. Due to utilization of the transformer, the output voltage of a push-pull converter can be either higher or lower than the input voltage. The push-pull converter is able to operate at a duty cycle close to 1.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | PWM signal Output 1 (MOSFET1 switch signal) |
| 7 | OUT2 | PWM signal Output 2 (MOSFET2 switch signal) |
| 2 | GND | Ground |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing (for current limit) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| IMAX | Maximum voltage on (external) current sensing resistor |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

➢ To view or change a component's model parameters:

1. Double-click on the placed component and select the **Value** tab.
2. Click **Edit Model** to display the **Edit Model** dialog box.
3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.4 PUSH_CM

The PUSH_CM is a generic model for Current Mode Push-Pull PWM controllers. A push-pull converter is an isolated version of buck converter. Due to utilization of the transformer, the output voltage of push-pull can be either higher or lower than the input voltage. Push-pull converters are able to operate at a duty cycle close to 1.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | PWM signal Output 1 (MOSFET1 switch signal) |
| 7 | OUT2 | PWM signal Output 2 (MOSFET2 switch signal) |
| 2 | GND | Ground |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing (for current limit) |
| 6 | VOSC | Oscillator ramp signal output (provided for ramp compensation purposes) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DEAD | Dead time between OUT1 and OUT2 |
| RAMP | Ramp amplitude for compensation |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.5 HALF_VM

The HALF_VM is a generic model for Voltage Mode Half-Bridge PWM controllers. The half-bridge converter is an isolated version of the buck converter. Due to the dual-switch configuration, it is able to handle larger power than other single-switch versions.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | PWM signal Output 1 (MOSFET1 switch signal) |
| 8 | GNF | Voltage reference for OUT2 |
| 7 | OUT2 | PWM signal Output 2 (MOSFET2 switch signal) |
| 2 | GND | Ground |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing (for current limit) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| DUTYMIN | Minimum duty cycle |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

➢ To view or change a component's model parameters:

1. Double-click on the placed component and select the **Value** tab.
2. Click **Edit Model** to display the **Edit Model** dialog box.
3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.6 HALF_CM

The HALF_CM is a generic model for Current Mode Half-Bridge PWM controllers. The half-bridge converter is an isolated version of the buck converter. Due to the dual-switch configuration, it can handle larger power than other single-switch versions.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | PWM signal Output 1 (SWITCH1 control signal) |
| 8 | GNF | Voltage reference for OUT2 |
| 7 | OUT2 | PWM signal Output 2 (Switch2 control signal) |
| 2 | GND | Ground |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing (for current limit) |
| 6 | VOSC | Oscillator ramp signal output (provided for ramp compensation purposes) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| RAMP | Ramp amplitude for compensation |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.7 FULL_CM

The FULL_CM is a generic model for Current Mode Full-bridge PWM controllers. The full-bridge converter is derived from the buck converter. By utilizing four operated switches, it is able to deliver a larger amount of power.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | PWM signal Output 1 (Switch1 control signal) |
| 8 | GNF1 | Voltage reference for OUT1 |
| 7 | OUT2 | PWM signal Output 2 (Switch2 control signal) |
| 2 | GND | Ground (Voltage reference for OUT2 and OUT4) |
| 9 | OUT3 | PWM signal Output 3 (Switch3 control signal) |
| 16 | GNF3 | Voltage reference for OUT3 |
| 15 | OUT4 | PWM signal Output 4 (Switch4 control signal) |
| 3 | COMP | Error amplifier output |

| Pin No. | Pin Name | Description |
|---|---|---|
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing (for current limit) |
| 6 | VOSC | Oscillator ramp signal output (provided for ramp compensation purposes) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| RAMP | Ramp amplitude for compensation |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.8 FULL_VM

The FULL_VM is a generic model for Voltage Mode Full-Bridge PWM controllers. The full-bridge converter is derived from the buck converter. By utilizing four operated switches, it is able to deliver a larger amount of power.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | PWM signal Output 1 (Switch1 control signal) |
| 8 | GNF1 | Voltage reference for OUT1 |
| 7 | OUT2 | PWM signal Output 2 (Switch2 control signal) |
| 2 | GND | Ground (Voltage reference for OUT2 and OUT4) |
| 9 | OUT3 | PWM signal Output 3 (Switch3 control signal) |
| 16 | GNF3 | Voltage reference for OUT3 |
| 15 | OUT4 | PWM signal Output 4 (Switch4 control signal) |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing (for current limit) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| DUTYMIN | MInimum duty cycle |
| RAMP | Ramp amplitude for compensation |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.1.9 2SWITCHCM

The 2SWITCHCM is a generic model for two-switch Current Mode PWM controllers. This is the two-switch version of PWMCM, which provides only one driver signal for single-switch converters.

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | PWM signal Output 1 (MOSFET switch1 signal) |
| 8 | GNF | Voltage reference for OUT1 |
| 7 | OUT2 | PWM signal Output 2 (MOSFET switch2 signal) |
| 2 | GND | Ground |
| 3 | COMP | Error amplifier output |
| 4 | FB | Output voltage feedback input |
| 5 | ISENSE | Switch current sensing |
| 6 | VOSC | Oscillator ramp signal output (provided for ramp compensation purposes) |

Generic PWM controller parameters:

| Parameter | Description |
|---|---|
| REF | Internal reference voltage |
| PERIOD | Switching period |
| DUTYMAX | Maximum duty cycle |
| RAMP | Ramp amplitude for compensation |
| VOUTHI | Driver output voltage high |
| VOUTLO | Driver output voltage low |
| ROUT | Driver output resistor |
| RATIO | Coefficient to scale the error signal |

Internal error amplifier parameters:

| Parameter | Description |
|---|---|
| VHIGH | Maximum output voltage |
| VLOW | Minimum output voltage |
| ISINK | Current sink capability |
| ISOURCE | Current source capability |
| POLE | First pole in Hertz |
| GAIN | DC open-loop gain (default = 90 dB) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2 SMPS Average Virtual

This component family contains a variety of averaged switched-mode power supplies (SMPS).

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

For more information about the components described in the following sections, refer to the Switch-Mode Power Supply SPICE Cookbook, McGraw-Hill, 2001.

## 12.2.1 BUCKCM

This is the averaged model (no switching component) of a basic buck converter in a current mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| OUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistor of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |

➢ To view or change a component's model parameters:

1. Double-click on the placed component and select the **Value** tab.
2. Click **Edit Model** to display the **Edit Model** dialog box.
3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.2 BUCKCCM

This is the Ripley's averaged model (no switching component) of a basic buck converter in a current mode controlled configuration. This is an improved model over BUCKCM, but it must operate in continuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |

➢ To view or change a component's model parameters:

1. Double-click on the placed component and select the **Value** tab.
2. Click **Edit Model** to display the **Edit Model** dialog box.
3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.3 BOOSTCCM

This is the Ripley's averaged model (no switching component) of a basic boost converter in a current mode controlled configuration. This is an improved model over BUCKCM, but it must operate in continuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.4 BOOSTCM

This is the averaged model (no switching component) of a basic boost converter in a current mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| OUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.5 BOOSTDCM

This is the Ripley's averaged model (no switching component) of a basic boost converter in a current mode controlled configuration. This is an improved model over BOOSTCM, but it must operate in discontinuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.6 BOOSTVM

This is the averaged model (no switching component) of a basic boost converter in a voltage mode controlled configuration.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.7 FLYBACKCCM

This is the Ripley's averaged model (no switching component) of a flyback converter in a current mode controlled configuration. This is an improved model over FLYBACKCM, but it must operate in continuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.8 BUCKDCM

This is the Ripley's averaged model (no switching component) of a basic buck converter in a current mode controlled configuration. This is an improved model over BUCKCM, but it must operate in discontinuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/S) |
| RI | Current sense resistor |
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |

VR = 2 V

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.9 BUCKVM

This is the averaged model (no switching component) of a basic buck converter in a voltage mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| OUT | Output voltage |
| GND | Ground |
| DON | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistor of output capacitor |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.10 FLYBACKCM

This is the averaged model (no switching component) of a basic flyback converter in a current mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| OUT | Output voltage |
| GND | Ground |
| CONTROL | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.11 FLYBACKDCM

This is the Ripley's averaged model (no switching component) of a flyback converter in a current mode controlled configuration. This is an improved model over FLYBACKCM, but it must operate in discontinuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| LS | Secondary inductance |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |
| N | Primary sensing versus secondary coil ratio |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.12FLYBACKVM

This is the averaged model (no switching component) of a basic flyback converter in a voltage mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| OUT | Output voltage |
| GND | Ground |
| DON | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.13 FWDCCM

This is the Ripley's averaged model (no switching component) of a forward converter in a current mode controlled configuration. This is an improved model over FORWARD_CM, but it must operate in continuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |

| Parameter | Description |
|---|---|
| RI | Current sense resistor |
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |
| N | Primary sensing versus secondary coil ratio |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.14 FORWARDCM

This is the averaged model (no switching component) of a basic forward converter in a current mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| OUT | Output voltage |
| GND | Ground |
| CONTROL | Feedback voltage error |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| LS | Secondary inductance |
| RS | Equivalent series resistor of output capacitor |
| MC | Compensation ramp (in V/S) |

| Parameter | Description |
|---|---|
| RI | Current sense resistor |
| N | Primary sensing versus secondary coil transformer ratio |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.15FWDDCM

This is the Ripley's averaged model (no switching component) of a forward converter in a current mode controlled configuration. This is an improved model over FORWARD_CM, but it must operate in discontinuous conduction mode.

| Pin Name | Description |
|---|---|
| VIN | Input voltage |
| VOUT | Output voltage |
| CONTROL | Feedback voltage error |
| GND | Ground |
| D | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| MC | Compensation ramp (in V/s) |
| RI | Current sense resistor |

| Parameter | Description |
|---|---|
| VOUT | Output voltage |
| VIN | Input voltage |
| RL | Load resistor |
| N | Primary versus secondary transformer ratio |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.16FORWARDVM

This is the averaged model (no switching component) of a forward converter in a voltage mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| OUT | Output voltage |
| GND | Ground |
| DON | Duty cycle setting |

| Parameter | Description |
|---|---|
| FS | Switching frequency |
| L | Main inductor |
| RS | Equivalent series resistance of output capacitor |
| N | Primary versus secondary transformer ratio |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.17 SEPICVM

This is the averaged model (no switching component) of a SEPIC (single-ended primary inductor converter) in a voltage mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| CS | Compensation capacitor to ground |
| GND | Ground |
| CP | Output and compensation capacitor to ground |
| DON | Duty cycle setting |

| Parameter | Description |
|---|---|
| RON | On resistance of switch |
| LP | Primary inductance value |
| LS | Secondary inductance value |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

# 12.2.18 SEPICCM

This is the averaged model (no switching component) of a SEPIC (single-ended primary inductor converter) in a current mode controlled configuration.

| Pin Name | Description |
|---|---|
| IN | Input voltage |
| CS | Compensation capacitor to ground |
| GND | Ground |
| CP | Output and compensation capacitor to ground capacitor |
| DON | Duty cycle setting |

| Parameter | Description |
|---|---|
| RON | On resistance of switch |
| LP | Primary inductance value |
| LS | Secondary inductance value |
| MC | Compensation ramp (V/s) |
| RI | Sense resistor |
| FS | Switching Frequency |

- To view or change a component's model parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. View or edit the model parameters as desired. For more information on the **Edit Model** dialog box, refer to the *Multisim User Guide*, or the Multisim helpfile.

## 12.2.19 ERRAMP

This device is a generic single pole op-amp.

- To edit this device's parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. Edit the **Current Instance Parameters** as desired.

## 12.2.20 AMPSIMP

This device is a generic single pole op-amp.

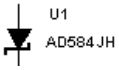
- To edit this device's parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. Edit the **Current Instance Parameters** as desired.

## 12.2.21 608PWM

This device is a generic pulse width modulator.

- To edit this device's parameters:
  1. Double-click on the placed component and select the **Value** tab.
  2. Click **Edit Model** to display the **Edit Model** dialog box.
  3. Edit the model as desired.

# 12.3 Voltage Reference




The output voltage of the Zener reference diode is set at approximately 6.9 V and requires a high voltage supply. The band-gap voltage reference diode has a significant advantage over the Zener reference diode in that it is capable of a lower minimum operating current and has a sharper knee.

The band-gap reference relies on matched transistors and is therefore easily integrated along with biasing, buffer and amplifier circuitry to give a complete reference diode.

The LM285/LM385 series are examples of micropower two-terminal band-gap voltage reference diodes. These devices are designed to operate over a wide current range of 10 µA to 20 mA.

The features of these devices include exceptionally low dynamic impedance, low noise, and stable operation over time and temperature. The low operating current make these devices suitable for micropower circuitry, such as portable instrumentation, regulators and other analog circuitry that requires extended battery life.

***Note*** Many types of two-terminal 1.2 V voltage reference diodes offer the same performance, but are not all directly interchangeable. Minor differences in regulation voltage and in allowable or required capacitive loading may affect a circuit.

# 12.4 Voltage Regulator

The linear IC voltage regulator is a device used to hold the output voltage from a dc power supply relatively constant over a wide range of line and load variations. Most commonly used IC voltage regulators are three-terminal devices.

There are four types of IC voltage regulators: fixed positive, fixed negative, adjustable, and dual tracking. The fixed-positive and fixed-negative IC voltage regulators are designed to provide specific output voltages. The adjustable regulator can be adjusted to provide any dc output voltage within two specified limits. The dual-tracking regulator provides equal positive and negative output voltages.

The regulator input-voltage polarity must match the device's rated output polarity regardless of the type of regulator used.

IC voltage regulators are series regulators, that is, they contain internal pass transistors and transistor control components. The internal circuitry of an IC voltage regulator is similar to that of the series feedback regulator.

## 12.4.1 Input/Output Voltage Differential Rating

The input/output voltage differential rating shows the maximum difference between $V_{in}$ and $V_{out}$ that can occur without damaging an IC voltage regulator.

The differential voltage rating can be used to determine the maximum allowable value of $V_{in}$ as follows:

$$V_{in(max)} = V_{out(adj)} + V_d$$

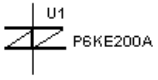
where:

$V_{in(max)}$ = the maximum allowable unrectified dc input voltage

$V_{out(adj)}$ = the adjusted output voltage of the regulator

$V_d$ = the input/output voltage differential rating of the regulator

# 12.5 Voltage Suppressor



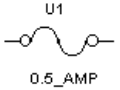

The voltage suppressor diode is a Zener diode that is capable of handling high surges. It is used as a filtering device to protect voltage-sensitive electronic devices from high energy voltage transients.

The voltage suppressor diode is connected across the AC power input line to a DC power supply. It contains two zener diodes that are connected back-to-back, making the voltage suppressor diode bi-directional. This characteristic enables it to operate in either direction to monitor under-voltage dips and over-voltage spikes of the AC input. It protects the power supply from surges by shorting out any voltages greater than the $V_z$ (Zener voltage) ratings of the diodes.

The voltage suppressor diode must also have extremely high power dissipation ratings because most AC power line surges contain a relatively high amount of power, in the hundreds of watts or higher. It must also be able to turn on rapidly to prevent damage to the power supply.

In DC applications, a single unidirectional voltage suppressor can be used instead of a bi-directional voltage suppressor. It is connected in shunt with the DC input and reverse biased (cathode to positive DC).

# 12.6 Fuse




This is a resistive component that protects against power surges and current overloads.

A fuse will blow (open) if the current in the circuit goes above $I_{max}$, the maximum current rating. $I_{max}$ can have any value from mA to kA.

The fuse is modeled by a resistor, *R*.

## 12.6.1 Characteristic Equations

$$R = 0 \qquad if \quad i_a \leq I_{max}$$
$$R = \infty \qquad if \quad i_a > I_{max}$$

where:

$i_a$ = current through the fuse, in amperes

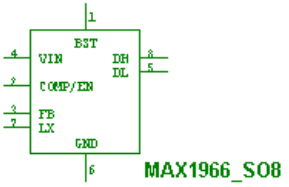
$I_{max}$ = maximum current rating of the fuse, in amperes.

For AC circuits, $I_{max}$ is the peak value of the current, not its RMS value.

## 12.6.2 Fuse Parameters and Defaults

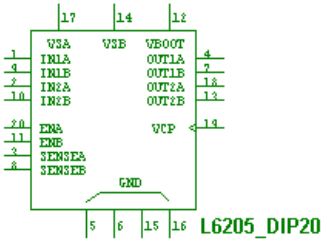
| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *Imax* | Maximum current | 1 | A |

# 12.7 PWM Controllers




This family contains footprint information for a number of components. Model data is not provided.

# 12.8 Miscellaneous Power



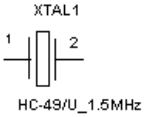

This family contains footprint information for a number of components. Model data is not provided.

# 12.9 Power Supply Controller

This family contains footprint information for a number of components. Model data is not provided.

# Chapter 13
# Misc. Components

## 13.1 Crystal




This component is made of pure quartz and behaves as a quartz crystal resonator, a circular piece of quartz with electrodes plated on both sides mounted inside an evacuated enclosure. When quartz crystals are mechanically vibrated, they produce an AC voltage. Conversely, when an AC voltage is applied across the quartz crystals, they vibrate at the frequency of the applied voltage. This is known as the piezoelectric effect and quartz is an example of a piezoelectric crystal.

The piezoelectric characteristics of quartz give the crystal the characteristics of a very high Q tuned circuit. The piezoelectric effect of quartz crystal links the mechanical and electrical properties of the resonator. Electrode voltage causes mechanical movement. Likewise, mechanical displacement generates an electrode voltage.

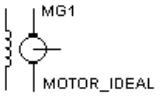
An equivalent circuit for a crystal shows a large inductor in series with a small resistance and a capacitance. When mounted in a holder with connections, a shunt capacitance is added to the equivalent circuit. The resultant equivalent circuit means that the crystal has both a series and parallel resonant frequency very close together.

Oscillators that employ crystals, typically quartz, offer excellent oscillation frequency stabilities of 0.001 percent. Crystal oscillators are used in digital wristwatches and in clocks that do not derive their frequency reference from the AC power line. They are also used in color television sets and personal computers. In these applications, one or more “quartz crystals” control frequency or time.

Another much more efficient transducer material than quartz is PZT. This ceramic material is ferroelectric and is made up of lead and other atoms, Ti or Zr. PZT consists of randomly

oriented crystallites of varying size. The piezoelectric but not the ferroelectric property of the ceramic materials of the PZT family is made use of in transducer applications, such as ultrasonic echo ranging (sonar), medical diagnostic ultrasound and nondestructive testing system devices.

# 13.2 DC Motor




The component is a universal model of an ideal DC motor which can be used to model the behavior of a DC motor excited in parallel, in series or separately. The excitation type of the component is determined by the interconnection of the terminals between field windings (terminals 1 and 2) and armature windings (terminals 3 and 4).

To excite the DC motor in parallel, connect the positive terminal of a DC source to terminals 2 and 4; then connect the negative terminals of the DC source to terminals 1 and 3. To excite the DC motor in series, connect terminal 2 to terminal 3 (use a connector); then connect the positive terminal of a DC source to terminal 4 and connect the negative terminal of the DC source to terminal 1. To excite the DC motor separately, connect a DC source to terminals 2 and 1 (positive and negative, respectively); then connect another DC source to terminals 4 and 3 (positive and negative, respectively).

Terminal 5 is the DC motor's output. The output is the motor's rpm value.

➢ To display this value:

- attach a voltmeter to terminal 5 (connect the other side of the voltmeter to ground) and simulate

or

- attach the oscilloscope to terminal 5 and simulate (the rpm value is the voltage that appears)

or

- attach a connector to terminal 5, then choose an appropriate analysis from the Analysis menu (for example, if you choose Analysis/DC Operating Point, the rpm value is the voltage at the connector).

This component connects the electrical and mechanical parts of a servo-system. Input to the motor is electrical while output is mechanical.

## 13.2.1 Characteristic Equations

The characteristic equations of an ideal DC motor are given by:

$$V_a = R_a * i_a + L_a \frac{di_a}{dt} + K_m * i_f * \omega_m$$

$$V_f = R_f * i_f + L_f \frac{di_f}{dt}$$

$$J \frac{d\omega_m}{dt} + B_f * \omega_m + T_L = K_m * i_f * i_a$$

where:

$\omega_m$ = rotational speed

$K_m$ = EMF constant

$V_a$ = armature voltage

$V_f$ = field voltage

Other terms are defined in “DC Motor Parameters and Defaults”.

The EMF constant $K_m$ is determined by:

$$K_m = \frac{V_{aN} - I_{aN} * R_a}{I_{fN} * \frac{2\pi * n_N}{60}}$$

where

$$I_{fN} = \frac{V_{fN}}{R_f}$$ for separately excited DC motor

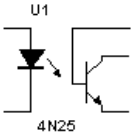
$$I_{fN} = \frac{V_{fN}}{R_f} = \frac{V_{aN}}{R_f}$$ for parallel excited DC motor

$$I_{fN} = \frac{V_{fN}}{R_f} = I_{aN}$$ for series excited DC motor

## 13.2.2 DC Motor Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *Ra* | Armature resistance | 1.1 | Ω |
| *La* | Armature inductance | 0.001 | H |
| *Rf* | Field resistance | 128 | Ω |
| *Lf* | Field inductance | 0.001 | H |
| *Bf* | Shaft friction | 0.01 | N m.s/rad |
| *J* | Machine rotational inertia | 0.01 | N.m.s$^2$/rad |
| *nn* | Rated rotational speed | 1800 | RPM |
| *Van* | Rated armature voltage | 115 | V |
| *Ian* | Rated armature current | 8.8 | A |
| *Vfn* | Rated field voltage | 115 | V |
| *Tl* | Load torque | 0.0 | N.m |

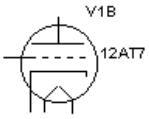
# 13.3 Optocoupler




An optocoupler is a device that uses light to couple a signal from its input (a photoemitter) to its output (a photodetector).

A typical optocoupler can be found in a six-pin dual in-line package (DIP) containing both an LED and a photodetector, and a transistor Darlington pair or SCR. The wavelength response of each device is structured to be as identical as possible to permit the highest measure of coupling possible.

# 13.4 Vacuum Tube




This component behaves as a three-electrode tube consisting of an anode, cathode and plate electrode. It is often used as an amplifier in audio applications.

The vacuum tube is a voltage controlled current device, very similar in operation to an N channel FET.

As for an FET, the gain of the tube is referred to as transconductance and is defined as the change in plate current resulting from a change in grid to cathode voltage:

gm = (change in plate current) / (change in grid to cathode voltage)

## 13.4.1 Characteristic Equations

The DC characteristic of the triode vacuum tube is modeled by a two-dimensional voltage-controlled current:

$$I_p = \begin{cases} K\left(\mu * V_{gk} + V_{pk}\right)^{\frac{3}{2}} & \text{for } \mu * \mathrm{V_{gk}} + \mathrm{V_{pk}} \geq 0 \\ 0 & \text{for } \mu * \mathrm{V_{gk}} + \mathrm{V_{pk}} < 0 \end{cases}$$

where

$$K = \frac{I_p}{\left(\mu * V_{gk} + V_{pk}\right)^{\frac{3}{2}}}$$

Other items are defined in “Triode Vacuum Tube Parameters and Defaults”.

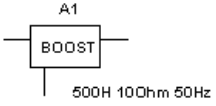
## 13.4.2 Model

The dynamic characteristic of the triode vacuum tube is modeled by its DC characteristic with three capacitances (Cgk, Cpk, and Cgp) which are associated interelectrodes.

## 13.4.3 Triode Vacuum Tube Parameters and Defaults

| Symbol | Parameter name | Default | Unit |
|---|---|---|---|
| Vpk | Plate-cathode voltage | 250 | V |
| Vgk | Grid-cathode voltage | -20 | V |
| Ip | Plate current | 0.01 | A |
| m | Amplification factor | 10 | - |
| Cgk | Grid-cathode capacitance | 2e-12 | F |
| Cpk | Plate-cathode capacitance | 2e-12 | F |
| Cgp | Grid-plate capacitance | 2e-12 | F |

# 13.5 Boost Converter




This component is an averaging circuit model that models the averaging behavior of a step-up DC-to-DC switching converter. It is based on a unified behavioral model topology. The topology models both small-signal and large-signal characteristics of this converter power stage. The model can be used to simulate DC, AC and large-signal transient responses of switched-mode power supplies operating in both the continuous and discontinuous inductor current conduction modes (CCM and DCM, respectively).

## 13.5.1 Characteristic Equations

The averaging DC and large-signal characteristics of a Boost converter are given by the following sets of equations:

$$I_i = I_{LL} + I_{LD} = I_L$$

$$I_0 = \frac{D2}{D+D2}\left(I_{LL} + I_{LD}\right) = \frac{D2}{D+D2} * I_L$$

in which $I_{LL}$ is governed by:

$$I_{LL} = \frac{1}{L}\int_0^t \left[D * V_i - D_2(V_0 - V_i)\right]dt$$

where $D$ = duty ratio of the switching device.

For the DCM:

$$D_2 = D * \frac{V_i}{V_0 - V_i}$$

$$V_l = 0$$

$$I_{LD} = \frac{D\left(D + D_2\right)}{2 * L * F_s} * V_i$$

For the critical condition between the CCM and the DCM of operations:

$$D_2 = 1 - D$$

$$I_{LD} = I_{Lcrit} = V_i * D * \frac{1}{2 * L * F_s}$$

For the CCM:

$$D_2 = 1 - D$$

$$V_L = D_i V_i - D_2\left(V_0 - V_i\right)$$

$$I_L = I_{Lcrit} + I_{LL}$$

The averaging behavior governed by the above equations is modeled using the built-in Multisim analog behavioral modeling components. The AC small-signal model is automatically computed inside the program.

## 13.5.2 Boost Converter Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *L* | Filter inductance | 500 | µH |
| *R* | Filter inductor ESR | 10 | mΩ |
| *Fs* | Switching frequency | 50 | kHz |

# 13.6 Buck Converter

This component is an averaging circuit model that models the averaging behavior of a step-down DC-to-DC switching converter. It is based on a unified behavioral model topology. The topology models both small-signal and large-signal characteristics of this converter power stage. The model can be used to simulate DC, AC and large-signal transient responses of switched-mode power supplies, operating in both the continuous and discontinuous inductor current conduction modes (CCM and DCM, respectively).

## 13.6.1 Characteristic Equations

The averaging DC and large-signal characteristics of a Buck converter are given by the following sets of equations:

$$I_i = \frac{D}{D + D_2} * (I_{LL} + I_{LD}) = \frac{D}{D + D_2} * I_L$$

$$I_o = -(I_{LL} + I_{LD}) = -I_L$$

in which $I_{LL}$ is governed by:

$$I_{LL} = \frac{1}{L} \int_0^t \left[ D(V_i - V_o) - D_2 V_0 \right] dt$$

where D = duty ratio of the switching device.

For the DCM:

$$D_2 = D\frac{V_i - V_0}{V_0}$$

$$V_l = 0$$

$$I_{LD} = D(V_i - V_0)\frac{D + D_2}{2 * L * F_s}$$

For the critical condition between the CCM and DCM of operation:

$$D_2 = 1 - D$$

$$I_{LD} = I_{Lcrit} = \frac{V_i - V_0}{2 * L * F_s}$$

For the CCM:

$$D_2 = 1 - D$$

$$V_L = D(V_i - V_0) - D_2 * V_o$$

$$I_L = I_{Lcrit} + I_{LL}$$

The averaging behavior governed by the above equations is modeled using the built-in Multisim analog behavioral modeling components. The AC small-signal model is automatically computed inside the program.

## 13.6.2 Buck Converter Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *L* | Filter inductance | 500 | µH |
| *R* | Filter inductor ESR | 5 | mΩ |
| *Fs* | Switching frequency | 50 | kHz |

# 13.7 Buck Boost Converter

This component is an averaging circuit model that models the averaging behavior of a DC-to-DC switching converter. It is based on a unified behavioral model topology. The topology models both small-signal and large-signal characteristics of this converter power stage. This behavioral model can be used to simulate DC, AC and large-signal transient responses of a variety of switched-mode power supplies, operating in both the continuous and discontinuous inductor current condition modes (DCM and CCM, respectively).

## 13.7.1 Characteristic Equations

$$I_i = \frac{D}{D + D_2} * (I_{LL} + I_{LD}) = \frac{D}{D + D_2} * I_L$$

$$I_o = \frac{D_2}{D + D_2} * (I_{LL} + I_{LD}) = \frac{D_2}{D + D_2} * I_L$$

in which $I_{LL}$ is governed by:

$$I_{LL} = \frac{1}{L} \int_0^t \left[ D * V_i - D_2 * V_o \right] dt$$

where D = duty ratio of the switching devices.

For the DCM:

$$D_2 = D \frac{V_i}{V_o}$$

$$V_L = 0$$

$$I_{LD} = \frac{D * V_i (D + D_2)}{2 * L * F_s}$$

For the critical condition between the CCM and the DCM of operation:

$$D_2 = 1 - D$$

$$I_{LD} = I_{Lcrit} = \frac{D * V_i}{2 * L * F_s}$$

For the CCM:

$$D_2 = 1 - D$$

$$V_L = D * V_i - D_2 * V_o$$

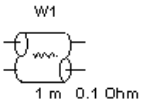
$$I_L = I_{Lcrit} + I_{LL}$$

The averaging behavior governed by these equations is modeled using Multisim's built-in analog behavioral modeling components. The AC small-signal model is automatically computed.

## 13.7.2 Buck-Boost Converter Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *L* | Filter inductance | 500 | µH |
| *R* | Filter inductor ESR | 5 | mW |
| *Fs* | Switching frequency | 50 | kHz |

# 13.8 Lossy Transmission Line




This component is a 2-port network that represents a medium, such as a wire or an interconnect, through which electrical signals pass.

The lossy model also models resistive losses in the line along with the characteristic impedance and propagation delay properties of the transmission line.

This is a two-part convolution model for single-conductor lossy transmission lines. The uniform constant-parameter distributed transmission line model can be used to model the following types of lines:

- RLC (uniform transmission lines with series loss only)
- RC (uniform RC lines)
- LC (lossless transmission lines)
- RG (distributed series and parallel conductance).

## 13.8.1 Model

The characteristic of a lossy transmission line is modeled by the Telegrapher Equations:

$$\frac{\partial v}{\partial x} = -(L\frac{\partial i}{\partial t} + Ri)$$

$$\frac{\partial i}{\partial x} = -(C\frac{\partial v}{\partial t} + Gv)$$

with the following boundary and initial conditions:

$v\ (0,t) = v_1(t),\ v\ (l,t) = v_2(t)$

$i\ (0,t) = i_1(t),\ i\ (l,t) = -i_2(t)$

$v\ (x,0) = v_0(x),\ i\ (x,0) = i_0(x)$

where the transmission line stretches from x coordinates 0 to l

$l$ = line length

$V(x,t)$ = voltage at point x at time t

$i\ (x,t)$ = current in the positive x direction at x at time t

$v\ (0,t)$ = voltage at point 0 at time t

$i\ (0,t)$ = current in the positive x direction at 0 at time t

$v\ (x,0)$ = voltage at point x at time 0

$i\ (x,0)$ = current in the positive x direction at x at time 0.

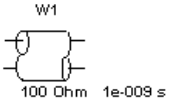
The set of equations is first transformed into a pair of coupled ordinary differential equations in x and s using the Laplace transformation. The equations are then reformulated for numerical convolution. Finally, inverse Laplace transforms are taken to return them to the time-domain form.

## 13.8.2 Lossy Transmission Line Model Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *Len* | Length of the transmission line | 100 | m |
| *Rt* | Resistance per unit length | 0.1 | Ω |
| *Lt* | Inductance per unit length | 1e-06 | H |
| *Ct* | Capacitance per unit length | 1e-12 | F |
| *Gt* | Conductance per unit length | 1e-12 | mho |
| *REL* | Breakpoint control | 1 | - |
| *ABS* | Breakpoint control | 1 | - |

***Note*** A lossy transmission line with zero loss can be used to model the lossless transmission line, and may be more accurate.

# 13.9 Lossless Line Type 1




This component is a 2-port network that represents a medium, such as a wire or an interconnect, through which electrical signals pass.

The lossless model is an ideal one that simulates only the characteristic impedance and propagation delay properties of the transmission line. The characteristic impedance is resistive and is equal to the square-root of L/C.

***Note*** A lossy transmission line with zero loss can be used to model the lossless transmission line, and may be more accurate.

## 13.9.1 Model

A lossless transmission line is an LC model.

The values of L and C are given by:

$$ct = \frac{td}{Z}$$

$$lt = td * Z$$

where:

*ct* = capacitance per unit length

*lt* = inductance per unit length

*td* = propagation time delay

*Z* = nominal impedance

The propagation time-delay may be calculated from the data-books as follows:

$$td = \left( \frac{length}{Vp} \right)$$

$$Vp = Vf * c$$

where:

*length* = length of the line

*Vp* = velocity of propagation

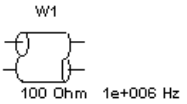
*Vf* = velocity-factor

*c* = speed of light

## 13.9.2 Lossless Transmission Line Model Parameters and Defaults

| Symbol | Parameter Name | Default | Unit |
|---|---|---|---|
| *Z0* | Nominal impedance | 100 | Ω |
| *Td* | Propagation time delay | 1e-09 | s |

## 13.9.3 Lossless Line Type 2

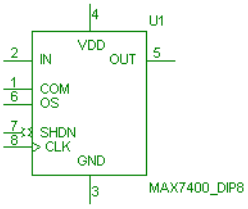



This component is similar to lossless line type 1.

# 13.10 Net

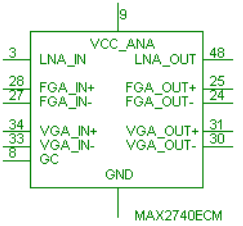
This is a template for building a model. It allows you to input a netlist, using from 2 to 20 pins.

# 13.11 Filters




A number of filters are included that have symbols for layout purposes. These have footprint, but no model information.

# 13.12 Miscellaneous Components




The MISC family contains footprint information for a number of components, for example, the Integrated GPS Receiver/Synthesizer shown here.

Model data is not provided.

# 13.13 MOSFET Driver

This family contains footprint information for a number of components. Model data is not provided.

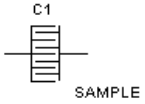
# 13.14 Filters

This family contains footprint information for a number of components. Model data is not provided.

# Chapter 14
# RF Components

RF components are not available in all editions of Multisim.

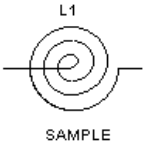
## 14.1 RF Capacitor




RF capacitors at RF frequencies show behaviors different from the regular capacitors at low frequencies. RF capacitors at RF frequencies act as a combination of a number of transmission lines, waveguides, discontinuities, and dielectrics. The dielectric layers are usually very thin (typically 0.2 Mμm). The equations governing these types of capacitors follow those of transmission lines; therefore, each RF capacitor is described by inductance per unit length, resistance per unit length, shunt capacitance per unit length, and shunt conductance per unit length. Depending on the type of the technology used, practical capacitance values are in the range between several picofarads and several nanofarads. These capacitors are used for coupling or bypassing for frequencies up to approximately 20 GHz.

One type of RF capacitor is called an interdigital capacitor. Both conductors of the capacitor are in the same plane, which is the top surface of the dielectric substrate used. Each conductor, or external node of the capacitor, is structured by connecting a number of transmission lines in parallel. In other words, the planar structure uses N thin parallel conducting strips of length L, linked alternately to one or other two strips of length W running perpendicularly alongside them, and the whole structure is deposited on a substrate, often of alumina. Capacitors of this type capacitors appear to be lumped up to 3 GHz and values from 0.1 to 10 pF can be achieved. However, because of their structure, they require a relatively large area.

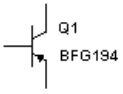
# 14.2 RF Inductor




From many types of RF inductors, spiral inductors provide higher inductance values and higher Qs. The spiral inductor is a technique of forming a planar inductor in a small place. The shape is described by an increasing radius with angle: i.e. $R = r/I + k\theta$

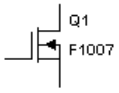
The equivalent circuit is a combination of series resistor (due to skin effect) and inductor, and shunt capacitors (due to the distance between the surface which embraces the conductor, and the ground plane). The quality of the inductor, usually noted as Q, is higher for spiral inductors than those of other types of inductors, such as the rectangular spiral.

# 14.3 RF Bipolar Transistors




Basic operation of an RF bipolar transistor is identical to that of transistors designed for low frequencies. RF transistors, however, have a higher maximum operating frequency ($W_t$), depending on base and collector transit and charging times. To achieve this, the physical size of emitter/base/collector areas at the layout level are minimized. However, reduction in the base area is limited by the technology used to fabricate the transistor. Reduction in the collector area is limited by the maximum tolerable voltage at the collector terminal. To achieve maximum power output, the emitter periphery area should be as large as possible. Because of these limitations, a special structure for bipolar transistors is used. This structure is commonly referred to as an interdigital bipolar transistor.

# 14.4 RF MOS_3TDN




RF FETs have a different type of carrier than bipolar transistors. Only the majority carriers selected for FET should have better transport properties (such as high mobility, velocity, diffusion coefficient). For this reason, RF FETs are fabricated on n-type materials since electrons have better properties.

The two most important parameters are the gate length and width. A reduction in the gate length will improve the gain, noise figure and frequency of operation. Increasing the gate width will increase the RF power capability. That is why typical power FETs have multiple gate fingers, interconnected via air bridges, with a total width of about 400 to 1000 µm.

The model parameters for RF FET transistors can be obtained using measured data for DC and RF S-parameters. The equivalent circuit model should have almost identical DC and RF S-parameters.

# 14.5 Tunnel Diode

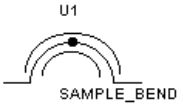



A tunnel diode is a heavily doped diode that is used in high-frequency communications circuits for applications such as amplifiers, oscillators, modulators, and demodulators. The unique operating curve of the tunnel diode is a result of the heavy doping used in the manufacturing of the diode. The tunnel diode is doped about one thousand times as heavily as standard *pn*-junction diode.

The tunnel diode is different from any other diode because of its negative-resistance region. In this area, forward voltage and current are inversely proportional. For example, an increase in forward voltage would result in a reduction in diode current.

A tunnel diode can also be used to generate a sinusoidal voltage using a DC supply and a few passive elements.

# 14.6 Strip Line




Stripline is one of the most commonly used transmission lines at microwave frequencies. Stripline is coined for ground-conductor-ground transmission line with a dielectric (normally air) in between. Due to the multiplicity of the circuit functions, substrate, technologies, and frequency bands, there is a wide range of stripline conductors. For example, microstrip lines are a special type of stripline where the upper ground is placed at infinity. Depending on the position of the stripline conductors, the shape of the conductor, and the thickness of the conductor, the equations governing the behavior of one stripline to another differ. For example, the centered stripline (often called Tri-Plate line), is a stripline where the conductance is placed symmetrically in each position (from top, bottom, left, and right). Another example is the Zero-Thickness stripline which is a very good approximation for striplines in which the thickness of the conductor is negligible compared to the distance it has from the ground planes.

# 14.7 Ferrite Beads



Ferrite beads are used for decoupling (blocking unwanted signals) on DC supply and some signal lines. They also provide attenuation of selected frequency bands.

The physical shape of a bead is similar to a toroid, but the bead has greater length to diameter ratio and usually a greater outside to inside diameter ratio than most toroid cores. Where the length to diameter ratio is even greater, the bead is often referred to as a sleeve. Different size/shape beads of the same material have different degrees of suppression. When used in conjunction with a bypass capacitor, a ferrite bead can provide extremely good decoupling.

# Chapter 15
# Electromechanical Components

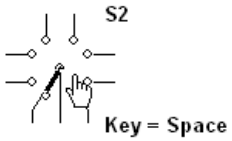
## 15.1 Sensing Switches




Sensing switches are interactive components that can be closed or opened (turned on or off) by pressing a key on the keyboard, or by using the mouse.

- To specify the key that controls the switch:
  1. Double-click on the switch and select its **Value** tab.
  2. Select the key in the **Key for Switch** drop-down list and click **OK**.
- To toggle the switch on or off using the keyboard, press the identified key.
- To toggle the switch on or off using the mouse, hover the cursor over the switch's arm and click when the arm takes on a thickened appearance.

## 15.2 Supplementary Contacts



This component family contains a variety of electromechanical switches. These switches are interactive components that can be closed or opened (turned on or off) by pressing a key on the keyboard, or by using the mouse.

- To specify the key that controls the switch:
  1. Double-click on the switch and select its **Value** tab.
  2. Select the key in the **Key for Switch** drop-down list and click **OK**.
- To toggle the switch on or off using the keyboard, press the identified key.
- To toggle the switch on or off using the mouse, hover the cursor over the switch's arm and click when the arm takes on a thickened appearance.

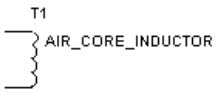
# 15.3 Momentary Switches




Momentary switches are interactive components that can be activated by pressing a key on the keyboard, or by using the mouse.

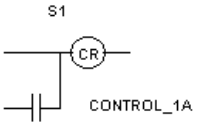
- To specify the key that controls the switch:
  1. Double-click on the switch and select its **Value** tab.
  2. Select the key in the **Key for Switch** drop-down list and click **OK**.
- To activate the switch using the keyboard, start the simulation and press the identified key. The switch changes state and then returns to its initial state.
- To toggle activate the switch using the mouse, hover the cursor over the switch's arm and click when the arm takes on a thickened appearance. The switch changes state and then returns to its initial state.

# 15.4 Line Transformer



Line Transformers are simplified transformers intended for power applications where the primary coils is connected to either 120 or 220 VAC. They will perform step up or step down functions plus several specialized functions of voltage and current measurement.

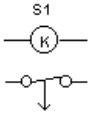
# 15.5 Coils, Relays




Multisim includes the following coils and relays:

- motor starter coil
- forward or fast starter coil
- reverse starter coil
- slow starter coil
- control relay
- time delay relay.

# 15.6 Timed Contacts



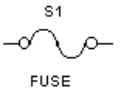

Multisim includes the following timed contacts:

- normally open timed open
- normally open timed closed
- normally closed timed open
- normally closed timed closed

➢ To change a timed contact's value:

1. Double-click on the placed component and click on the **Value** tab.
2. Change the desired parameters (for example, **Delay Time**) and click **OK** to close the component's properties dialog.

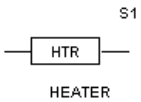
# 15.7 Protection Devices




Multisim includes the following protection devices

- fuse
- overload
- overload thermal
- overload magnetic
- ladder logic overload

# 15.8 Output Devices




Multisim includes the following output devices:

- light indicator
- motor
- DC motor armature
- 3 phase motor
- heater
- LED indicator
- solenoid.

# 15.9 Pilot Lights

Multisim includes the following pilot lights:

- non push-to-test
- push-to-test.

# 15.10 Terminals

Multisim includes the following terminals:

- power terminals
- control terminals N.O.
- control terminals N.C.
- coil terminals.

# Appendix A

## A.1 Technical Support and Professional Services

Visit the following sections of the National Instruments web site at ni.com for technical support and professional services:

- **Support** — online technical support resources at ni.com/support include the following:
  - **Self-Help Resources** — For answers and solutions, visit the award-winning National Instruments web site for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on.
  - **Free Technical Support** — All registered users receive free Basic Service, which includes access to hundreds of Application Engineers worldwide in the NI Discussion Forums at ni.com/forums. National Instruments Application Engineers make sure every question receives an answer. For information about other technical support options in your area, visit ni.com/services or contact your local office at ni.com/contact.
- **Training and Certification** — Visit ni.com/training for self-paced training, eLearning, virtual classrooms, interactive CDs, and Certification program information. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration** — If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed in the front of this manual. You can also visit the Worldwide Offices section of ni.com/niglobal to access the branch office web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

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